MOTOROLA

SN54/74LS490

DUAL DECADE COUNTER

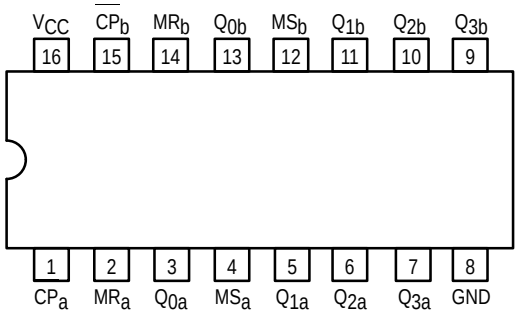
The SN54/74LS490 contains a pair of high-speed 4-stage ripple counters. Each half of the SN54/74LS490 has individual Clock, Master Reset and Master Set (Preset 9) inputs. Each section counts in the 8, 4, 2, 1 BCD code.

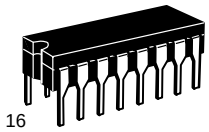
- Dual Version of SN54/74LS490
- Individual Asynchronous Clear and Preset to 9 for Each Counter
- Count Frequency — Typically 65 MHz
- Input Clamp Diodes Limit High-Speed Termination Effects

DUAL DECADE COUNTER

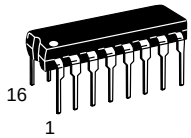
LOW POWER SCHOTTKY

CONNECTION DIAGRAM DIP (TOP VIEW)

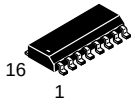




J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

PIN NAMES

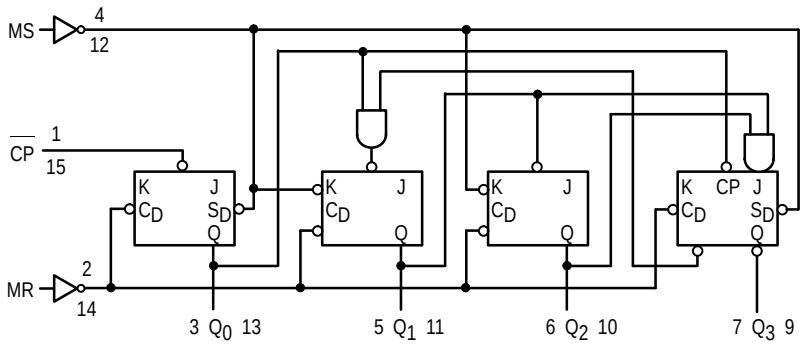
		LOADING (Note a) HIGH	LOW
MS	Master Set (Set to 9) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset	0.5 U.L.	0.25 U.L.
CP	Clock Input (Active LOW Going Edge)	1.5 U.L.	1.5 U.L.
$Q_0 - Q_3$	Counter Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC DIAGRAM (ONE HALF SHOWN)



TRUTH TABLE

COUNT	OUTPUTS Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			–0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	MS, MR			–0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		Clock			–1.6			
I_{OS}	Short Circuit Current (Note 1)		–20		–100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				26	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC SET-UP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_W	Any Pulse Width	20			ns	V_{CC} = 5.0 V
t_S	MR or MS to Setup Time	25			ns	

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
f_{MAX}	Maximum Clock Frequency	25	35		MHz	Figure 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_0		12 13	20 20	ns	Figure 1	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_1 or Q_3		24 26	39 39	ns	Figure 3	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_2		32 36	54 54	ns	Figure 2	
t_{PHL}	Propagation Delay, MR to Output		24	39	ns	Figure 2	
t_{PLH} t_{PHL}	Propagation Delay, MS to Output		24 20	39 36	ns	Figure 2	

AC WAVEFORMS

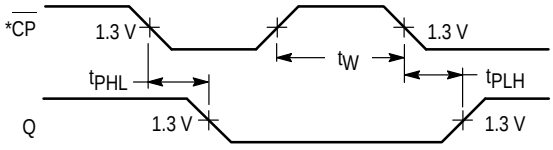


Figure 1

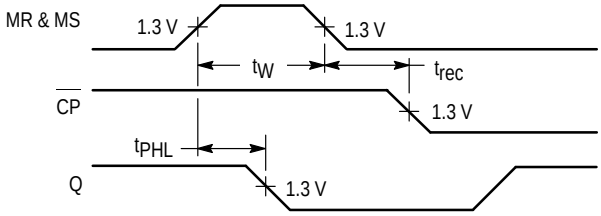


Figure 2

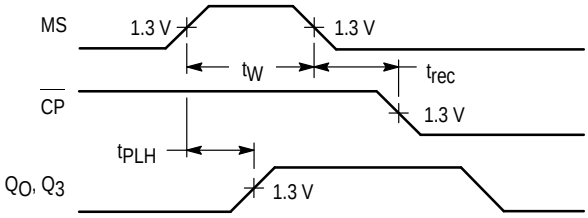


Figure 3

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the Truth Table.