SN54/74LS299

8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

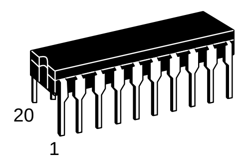
The SN54/74LS299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

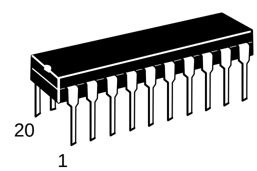
- Common I/O for Reduced Pin Count
- Four Operation Modes: Shift Left, Shift Right, Load and Store
- Separate Shift Right Serial Input and Shift Left Serial Input for Easy Cascading
- 3-State Outputs for Bus Oriented Applications
- Input Clamp Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

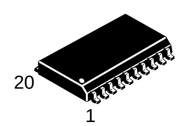
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03

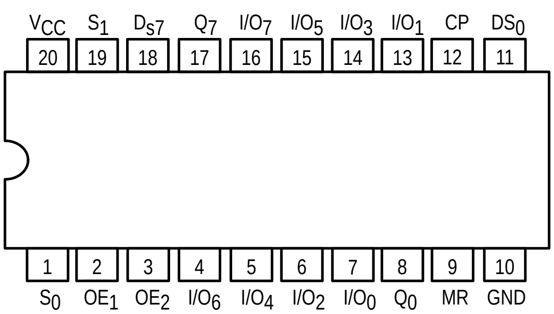


DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXDW	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)

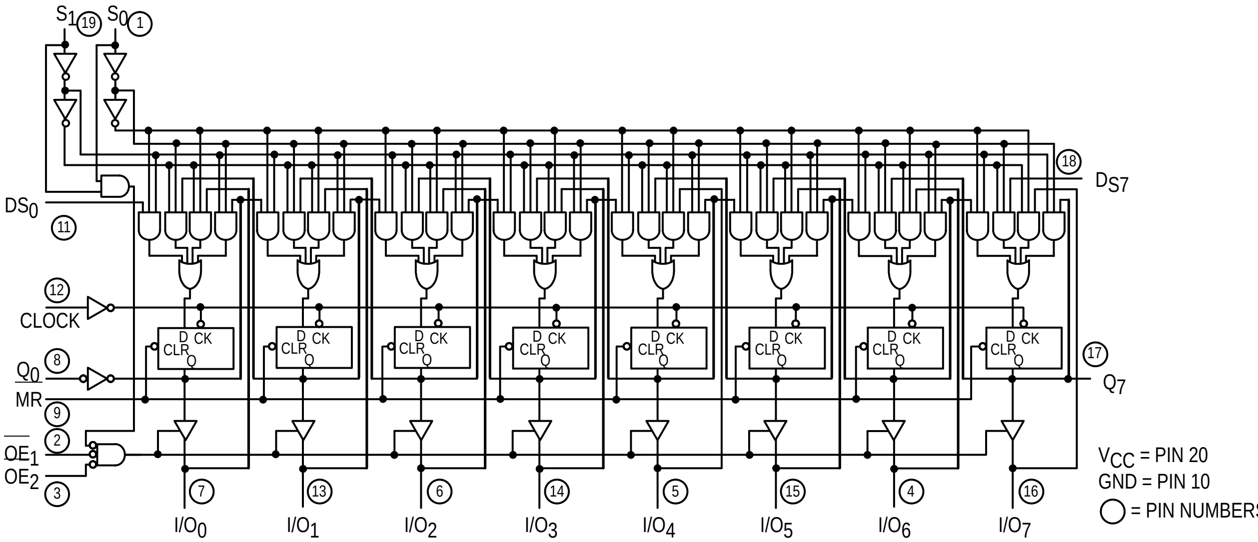


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a) HIGH	LOW
CP	Clock Pulse (active positive-going edge) Input	0.5 U.L.	0.25 U.L.
DS0	Serial Data Input for Right Shift	0.5 U.L.	0.25 U.L.
DS7	Serial Data Input for Left Shift	0.5 U.L.	0.25 U.L.
I/O_n	Parallel Data Input or	0.5 U.L.	0.25 U.L.
	Parallel Output (3-State) (Note c)	65 (25) U.L.	15 (7.5) U.L.
$\overline{OE_1}$, $\overline{OE_2}$	3-State Output Enable (active LOW) Inputs	0.5 U.L.	0.25 U.L.
Q_0, Q_7	Serial Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{MR}$	Asynchronous Master Reset (active LOW) Input	0.5 U.L.	0.25 U.L.
S_0, S_1	Mode Select Inputs	1 U.L.	0.5 U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
c) The Output LOW drive factor is 7.5 U.L for Military (54) and 15 U.L. for Commercial (74). The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS								RESPONSE
$\overline{MR}$	S_1	S_0	$\overline{OE_1}$	$\overline{OE_2}$	CP	DS_0	DS_7	
L	X	X	H	X	X	X	X	Asynchronous Reset; $Q_0 = Q_7$ = LOW
L	X	X	X	H	X	X	X	I/O Voltage Undetermined
L	H	H	X	X	X	X	X	
L	L	X	L	L	X	X	X	Asynchronous Reset; $Q_0 = Q_7$ = LOW
L	X	L	L	L	X	X	X	I/O Voltage LOW
H	L	H	X	X	↑	D	X	Shift Right; D→Q_0; Q_0→Q_1; etc.
H	L	H	L	L	↑	D	X	Shift Right; D→Q_0 & I/O_0; Q_0→O_1 & I/O_1; etc.
H	H	L	X	X	↑	X	D	Shift Left; D→Q_7; Q_7→Q_6; etc.
H	H	L	L	L	↑	X	D	Shift Left; D→Q_7 & I/O_7; Q_7→Q_6 & I/O_6; etc.
H	H	H	X	X	↑	X	X	Parallel Load; I/O_n→Q_n
H	L	L	H	X	X	X	X	Hold: I/O Voltage undetermined
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold: I/O_n = Q_n

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

Symbol	Parameter			Min	Typ	Max	Unit
V_{CC}	Supply Voltage		54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range		54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	Q_0, Q_7	54, 74			–0.4	mA
I_{OL}	Output Current — Low	Q_0, Q_7 Q_0, Q_7	54 74			4.0 8.0	mA
I_{OH}	Output Current — High	I/O_0–I/O_7 I/O_0–I/O_7	54 74			–1.0 – 2.6	mA
I_{OL}	Output Current — Low	I/O_0–I/O_7 I/O_0–I/O_7	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage $I/O_0–I/O_7$	54	2.4	3.2		V	V_{CC} = MIN, I_{OH} = MAX
		74	2.4	3.1		V	
V_{OH}	Output HIGH Voltage Q_0, Q_7	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = MAX
		74	2.7	3.4		V	
V_{OL}	Output LOW Voltage $I/O_0–I/O_7$	54, 74		0.25	0.4	V	I_{OL} = 12 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA
V_{OL}	Output LOW Voltage $I/O_0–I/O_7$	54, 74			0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74			0.5	V	I_{OL} = 8.0 mA
I_{OZH}	Output Off Current HIGH $I/O_0–I/O_7$				40	µA	V_{CC} = MAX, V_{OUT} = 2.7 V
I_{OZL}	Output Off Current LOW $I/O_0–I/O_7$				–400	µA	V_{CC} = MAX, V_{OUT} = 0.4 V
I_{IH}	Input HIGH Current	Others			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
		S_0, S_1, $I/O_0–I/O_7$			40	µA	
		Others			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
		S_0, S_1			0.2	mA	
		$I/O_0–I/O_7$			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current	Others			–0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
		S_0, S_1			–0.8	mA	
I_{OS}	Short Circuit Current (Note 1)	Q_0, Q_7	–20		–100	mA	V_{CC} = MAX
		$I/O_0–I/O_7$	–30		–130	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				53	mA	V_{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	25	35		MHz	C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, Clock to Q_0 or Q_7		26 22	39 33	ns	C_L = 15 pF
t_{PHL}	Propagation Delay, Clear to Q_0 or Q_7		27	40	ns	C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, Clock to $I/O_0-I/O_7$		26 17	39 25	ns	C_L = 45 pF, R_L = 667 Ω
t_{PHL}	Propagation Delay, Clear to $I/O_0-I/O_7$		26	40	ns	C_L = 45 pF, R_L = 667 Ω
t_{PZH} t_{PZL}	Output Enable Time		13 19	21 30	ns	C_L = 45 pF, R_L = 667 Ω
t_{PHZ} t_{PLZ}	Output Disable Time		10 10	15 15	ns	C_L = 5.0 pF

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_W	Clock Pulse Width HIGH	25			ns	V_{CC} = 5.0 V
t_W	Clock Pulse Width LOW	13			ns	V_{CC} = 5.0 V
t_W	Clear Pulse Width LOW	20			ns	V_{CC} = 5.0 V
t_s	Data Setup Time	20			ns	V_{CC} = 5.0 V
t_s	Select Setup Time	35			ns	V_{CC} = 5.0 V
t_h	Data Hold Time	0			ns	V_{CC} = 5.0 V
t_h	Select Hold Time	10			ns	V_{CC} = 5.0 V
t_{rec}	Recovery Time	20			ns	V_{CC} = 5.0 V

3-STATE WAVEFORMS

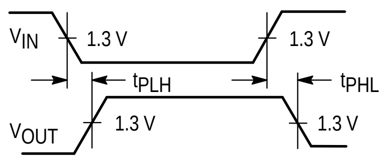


Figure 1

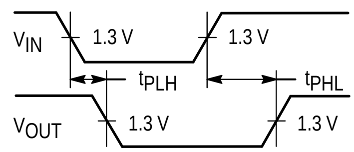


Figure 2

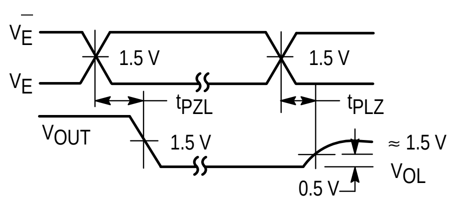


Figure 3

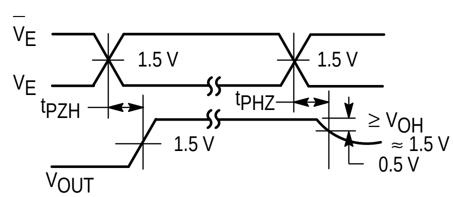
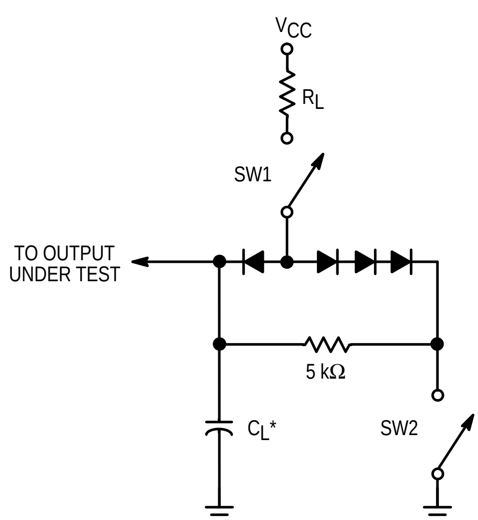


Figure 4

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Figure 5