

# Schematic Package Supplement to

# Kangaroo™

## Operation, Maintenance and Service Manual

**NOTE**

*This staple temporarily holds the schematic package together. Remove the staple before using the schematics.*



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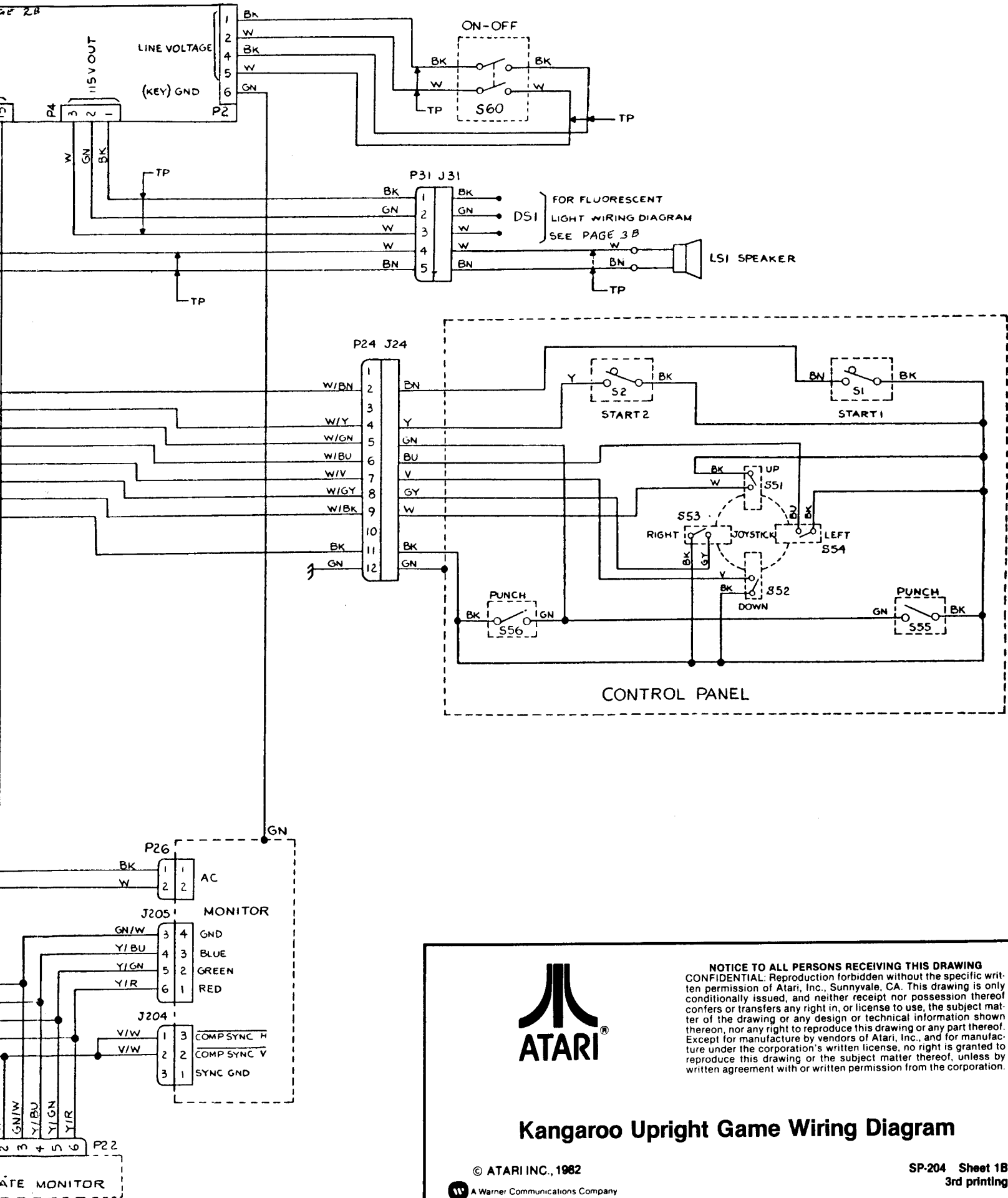
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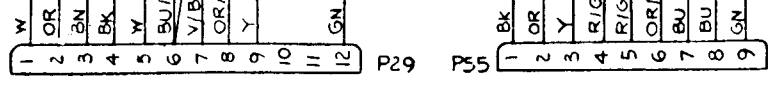
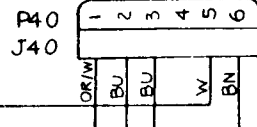
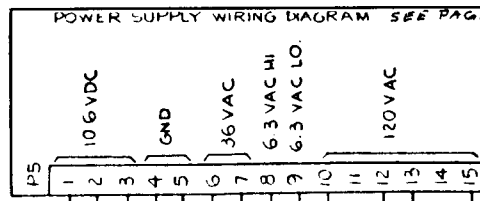
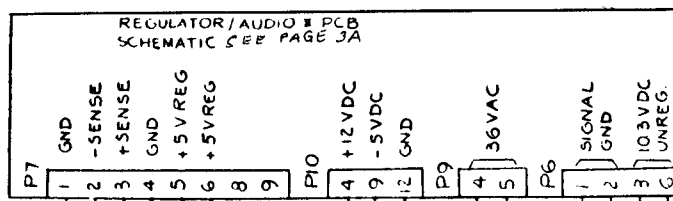
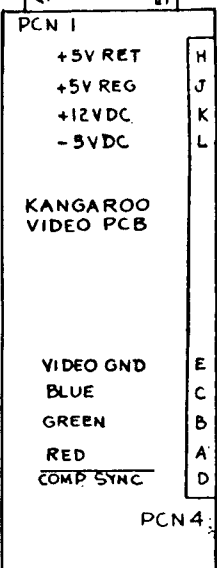
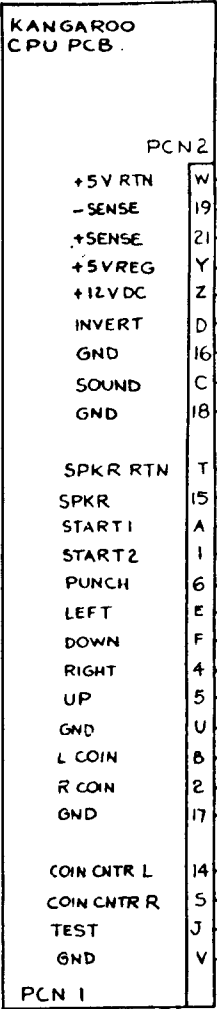
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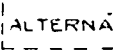


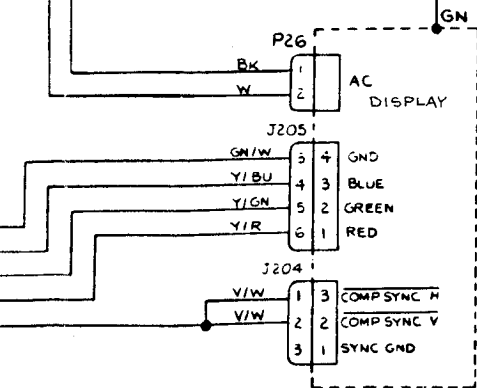
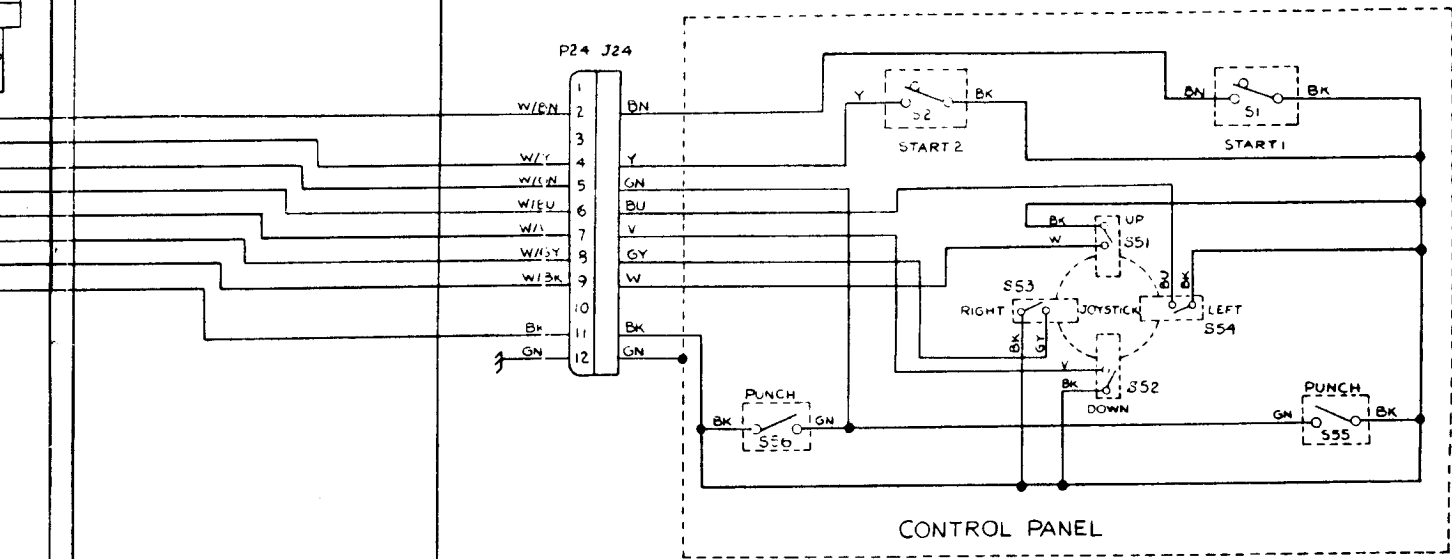
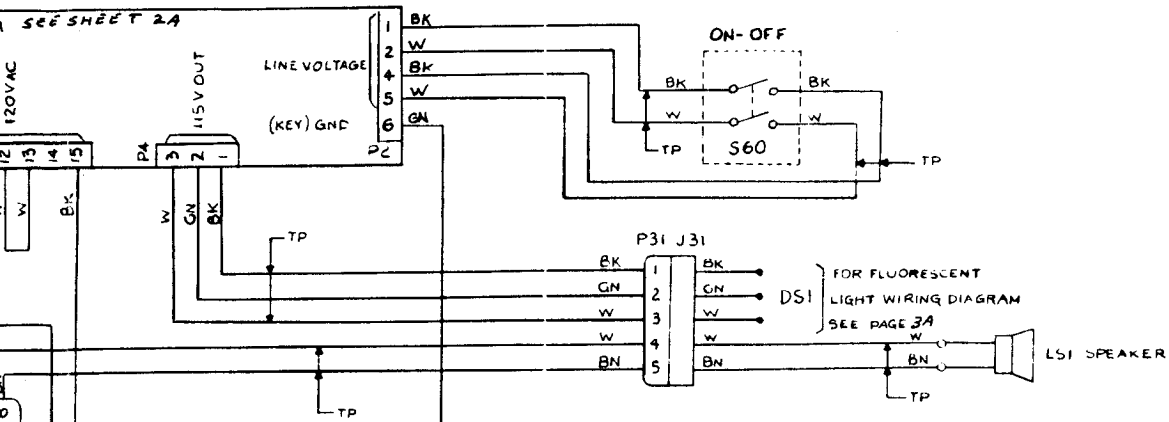
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FOR COMPONENT WIRING DIAGRAM SEE PAGE 3B

FOR COIN DOOR WIRING DIAGRAM SEE PAGE 3B





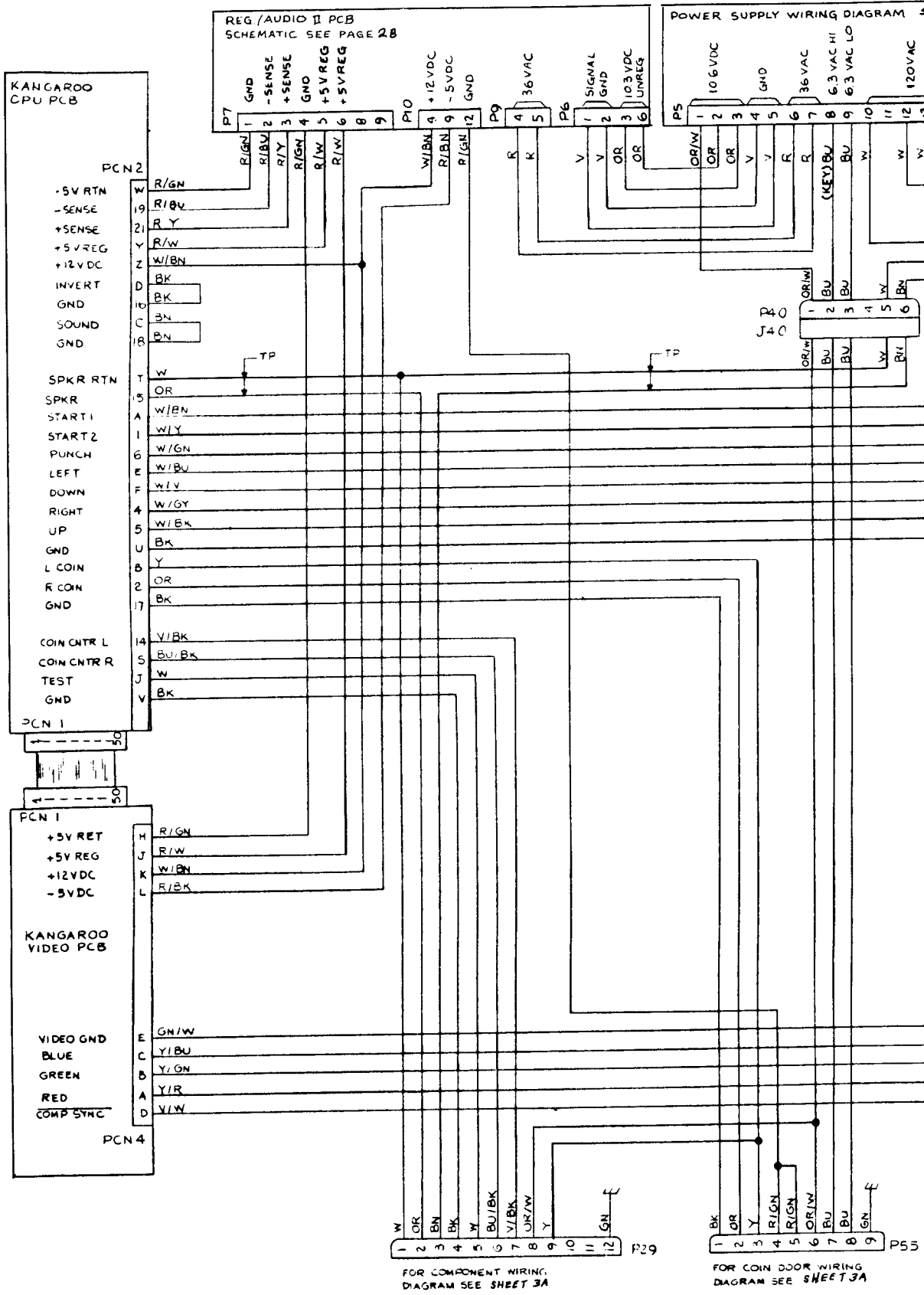
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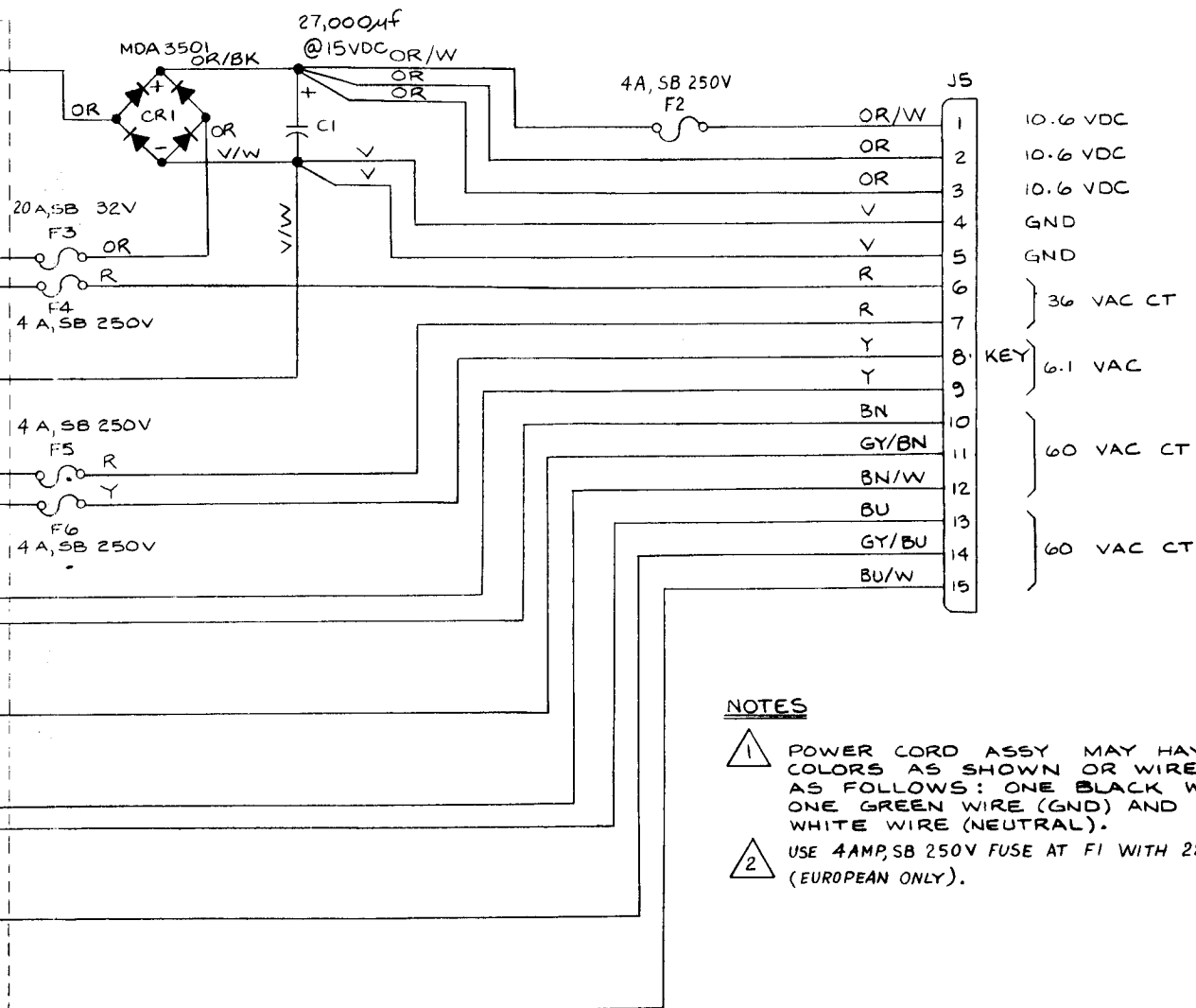
## Ireland-Built Kangaroo Game Wiring Diagram

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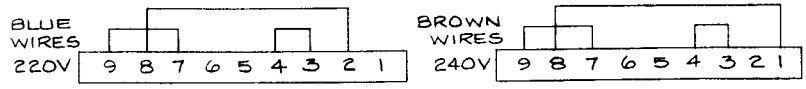
**NOTES**

- ⚠ 1 POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).
- ⚠ 2 USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY).

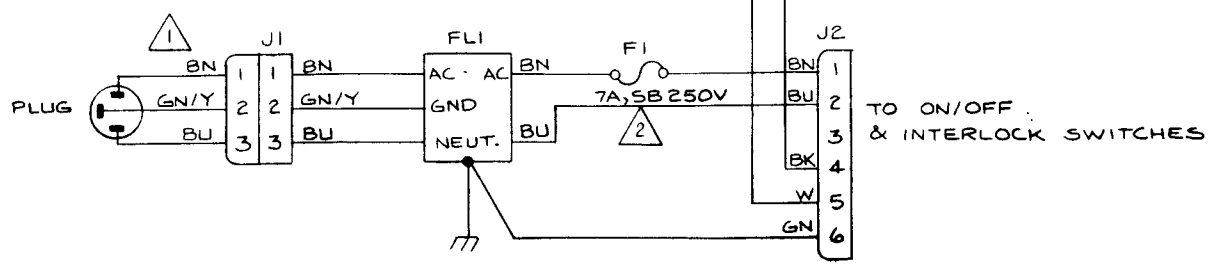
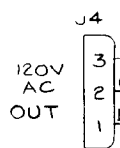
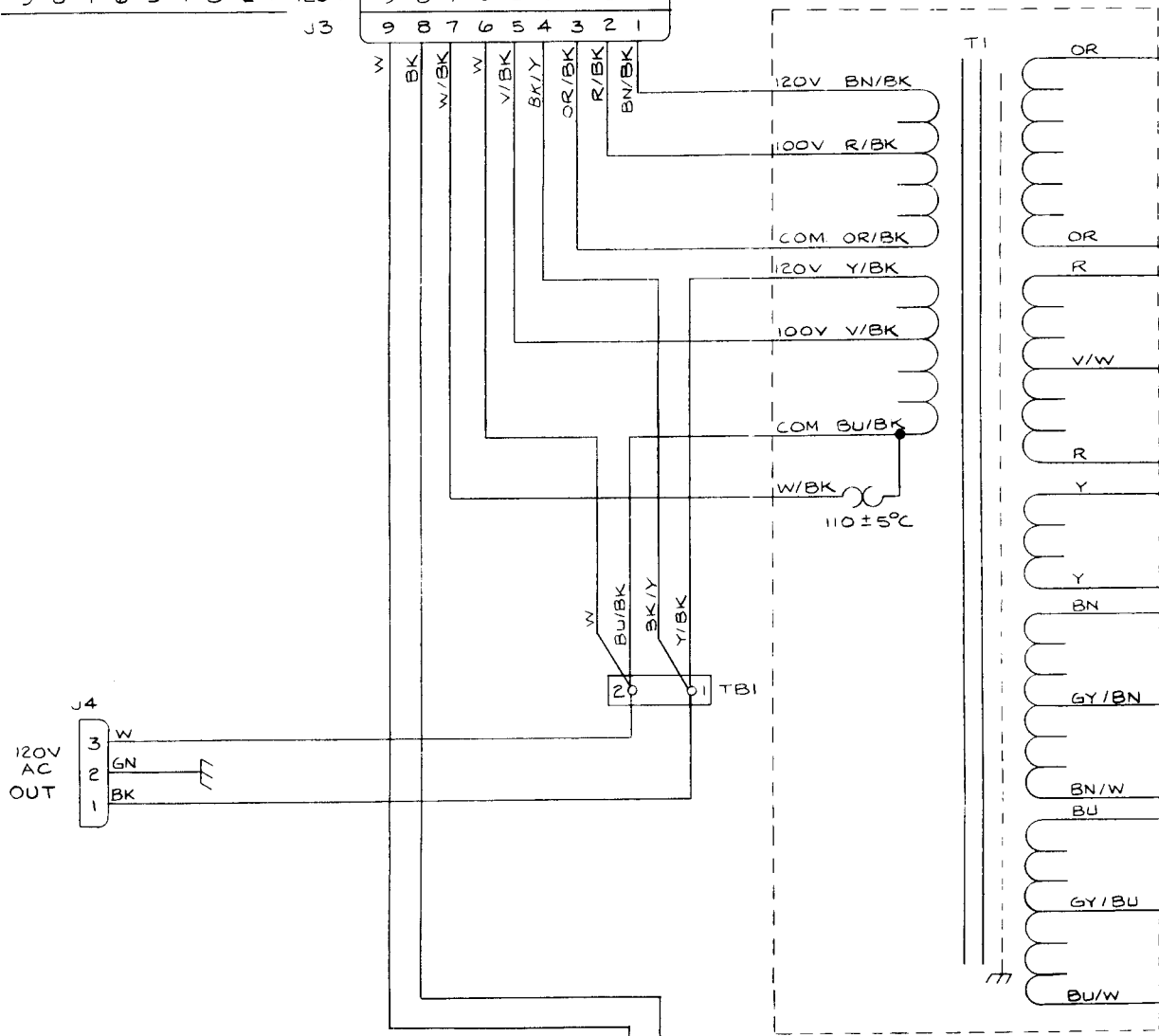
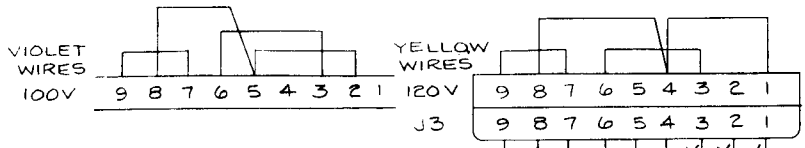


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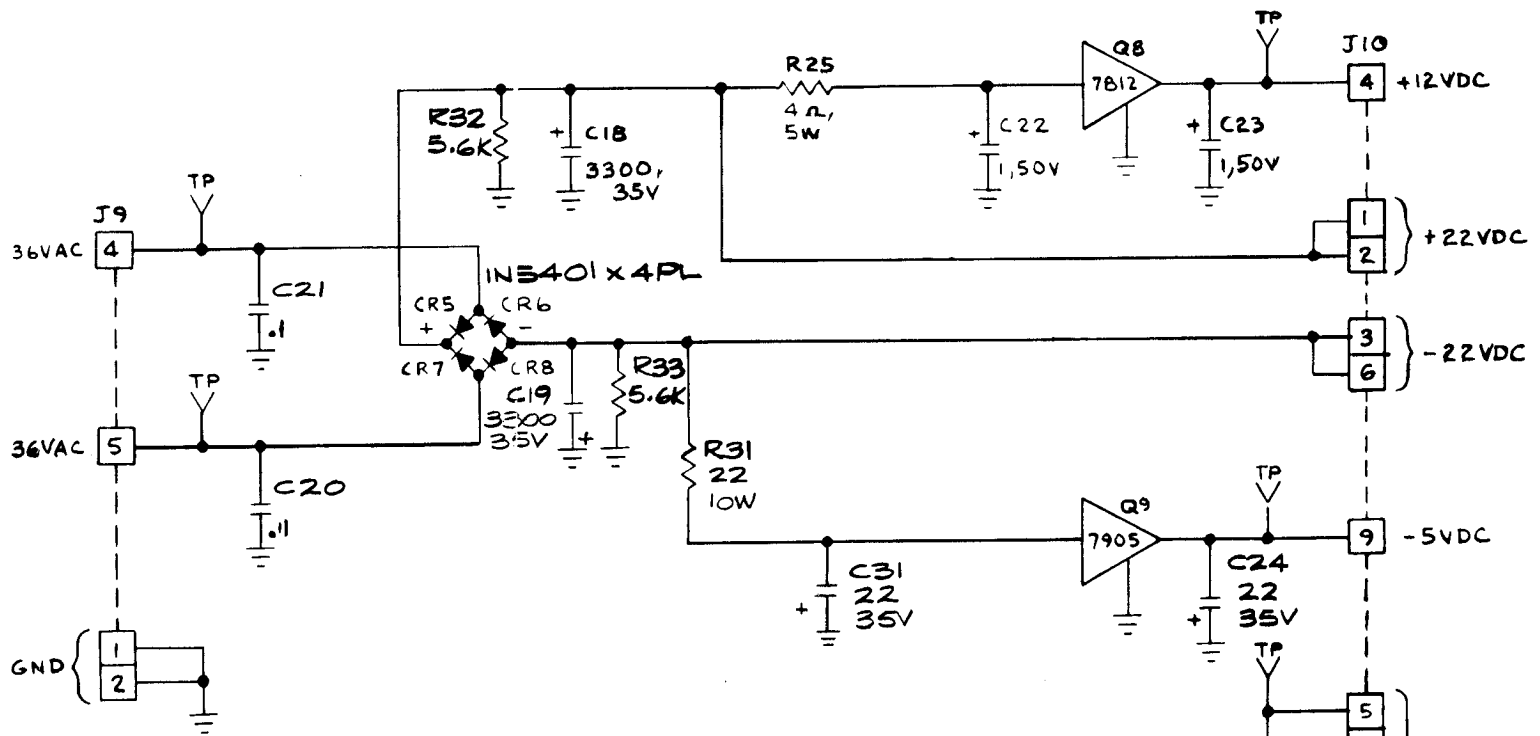
**Kangaroo Power Supply**



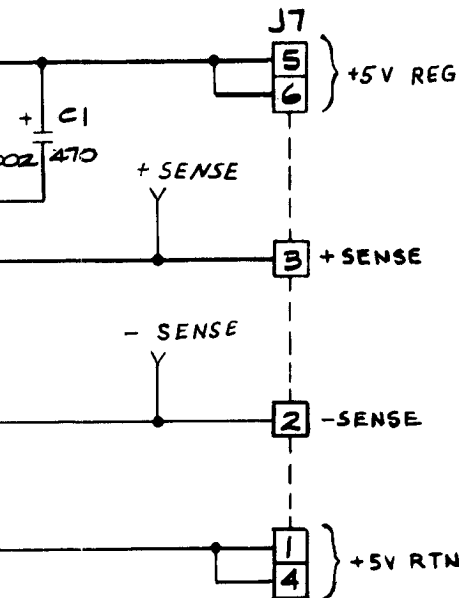
VOLTAGE SELECTION BLOCKS







| LAST DES | NOT USED                 |
|----------|--------------------------|
| C31      | C3-7, 9-12, 14-17, 25-30 |
| CR8      | CR2, 3                   |
| Q11      | Q10, 11, 4, 6            |
| R33      | R2, 9-23, 26-28          |



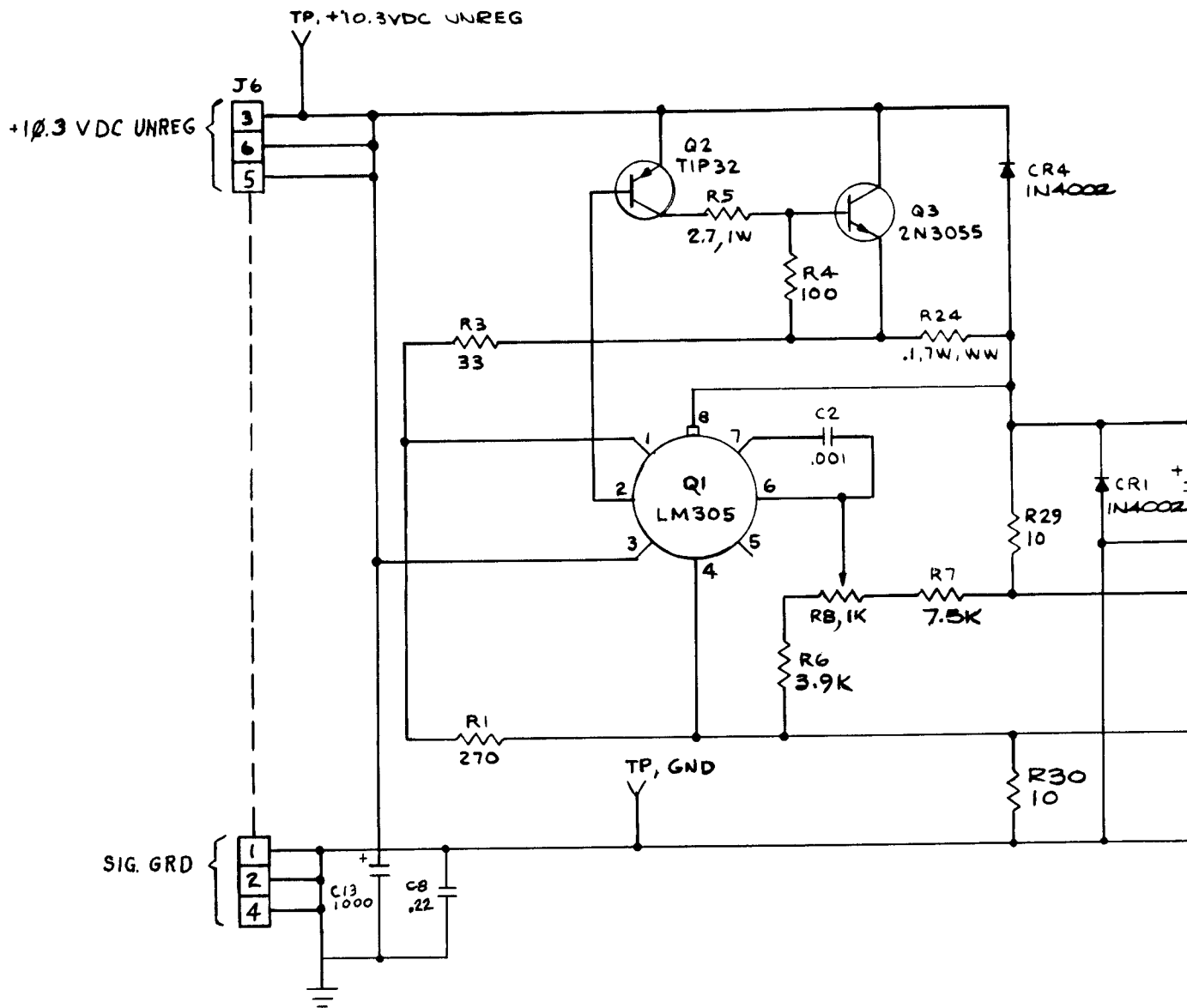
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## Kangaroo Reg./Audio II PCB Schematic Diagram

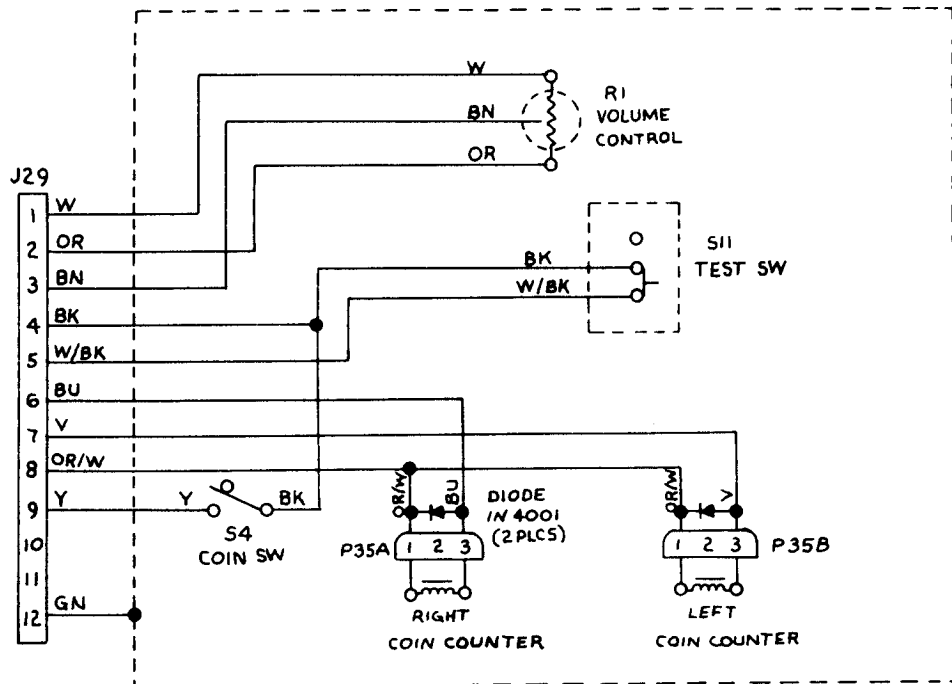
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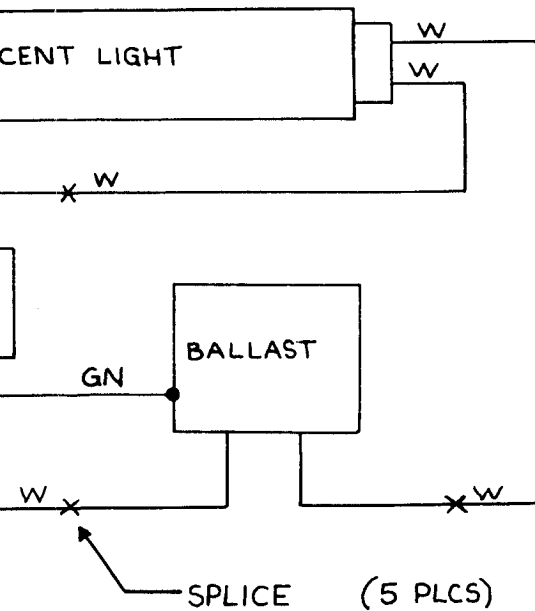
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## Utility Panel Wiring Diagram



## Speaker Wiring Diagram



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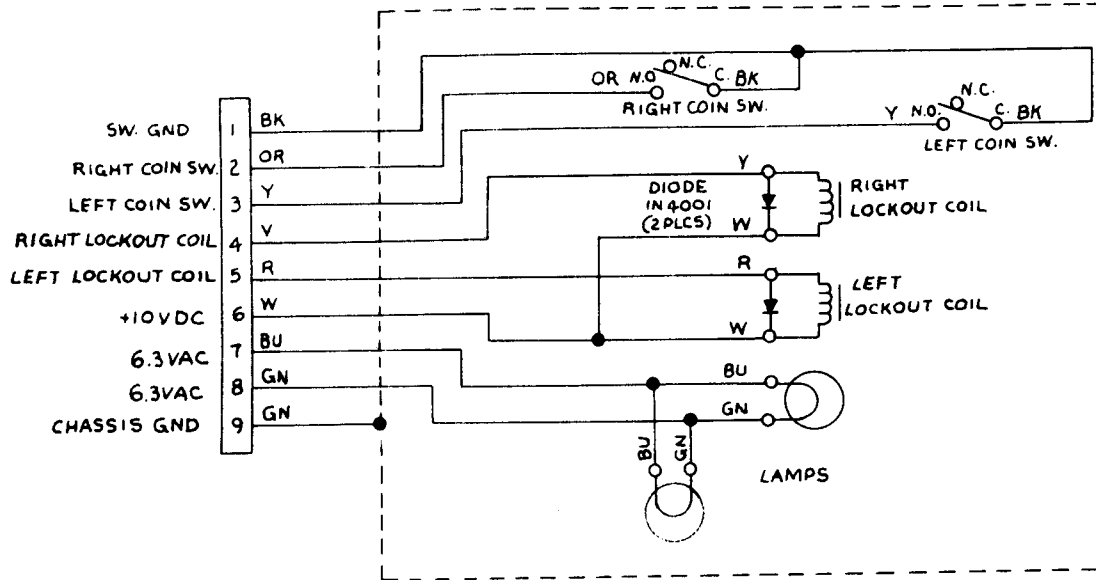
## Kangaroo Game Wiring Interfaces

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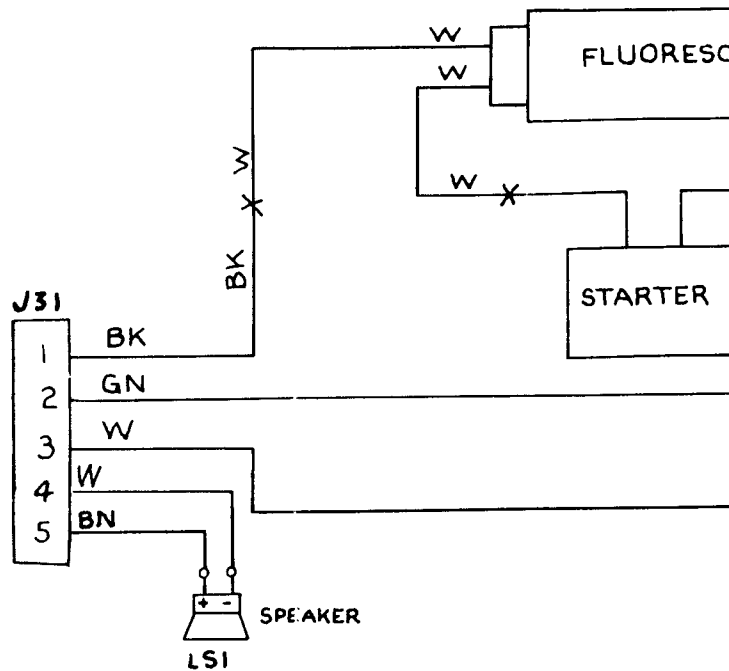
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## Coin Door Wiring Diagram

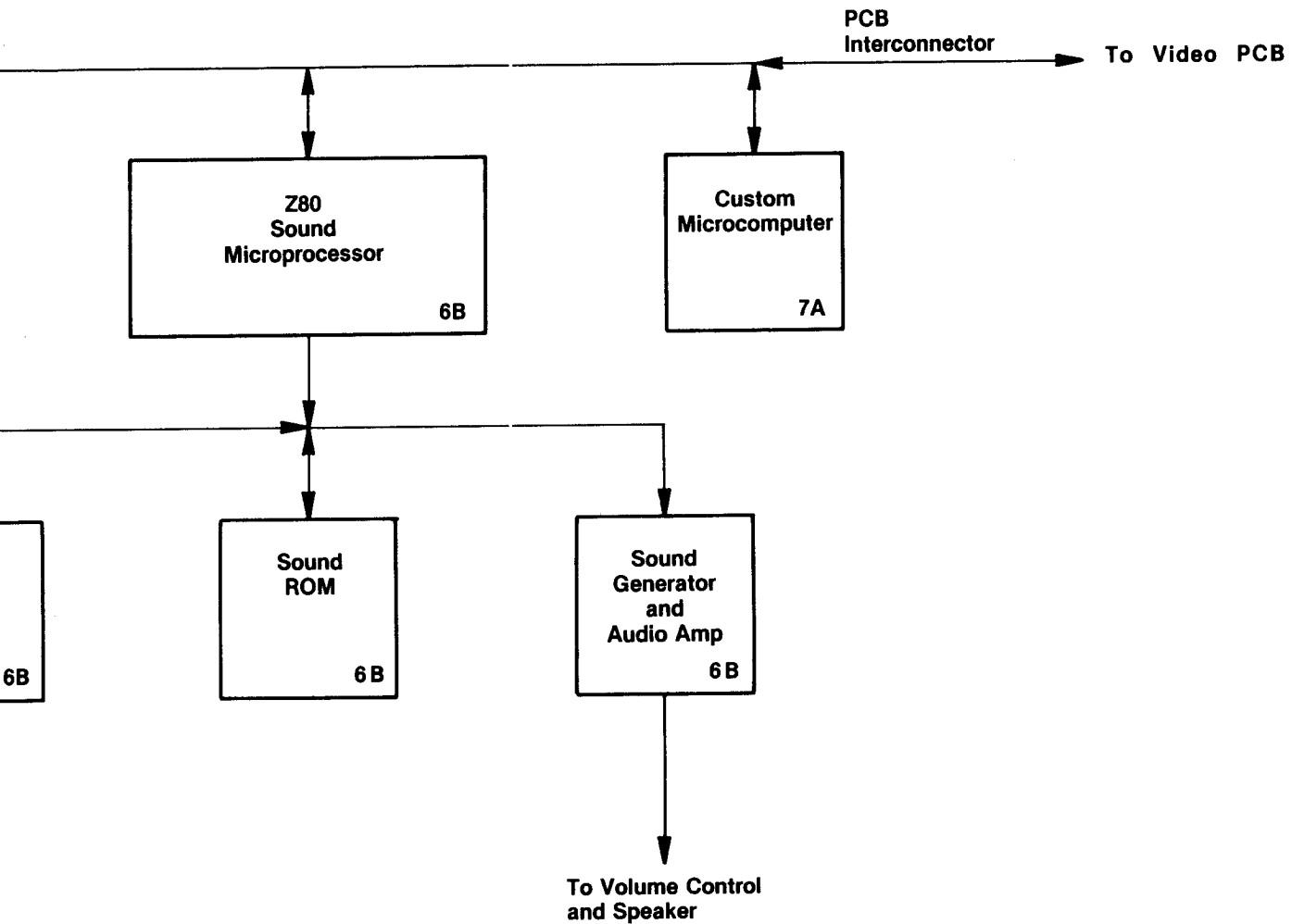


## Fluorescent Light and



# NOTE

The **service switch**, located on the CPU PCB, allows you to enter credits without tripping the coin counter.



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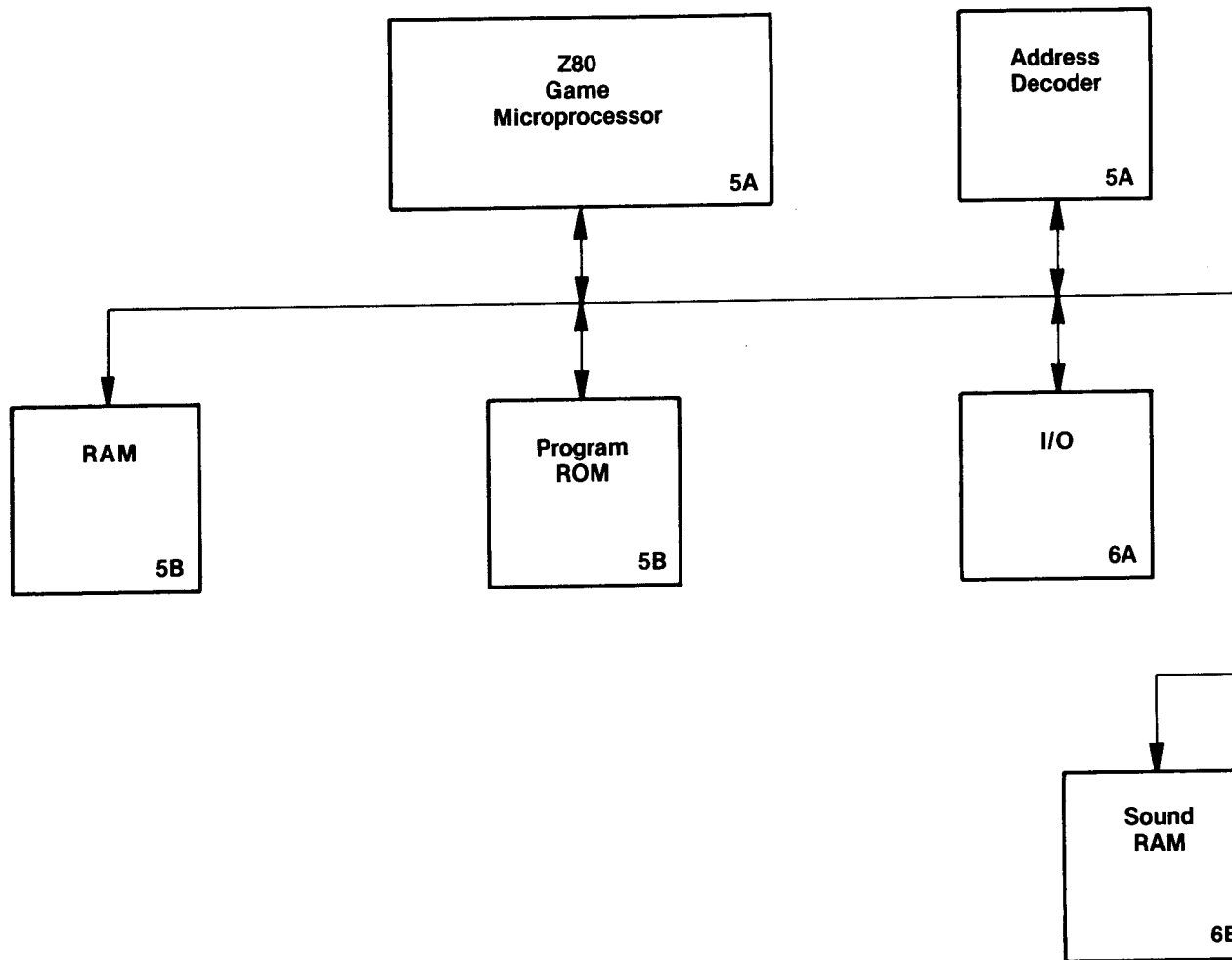
## Kangaroo CPU PCB Schematic Diagram

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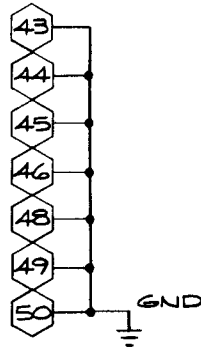
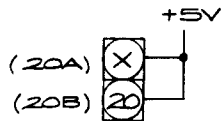
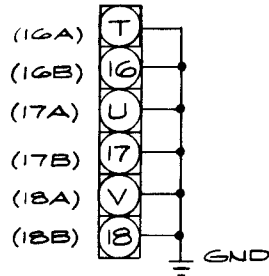
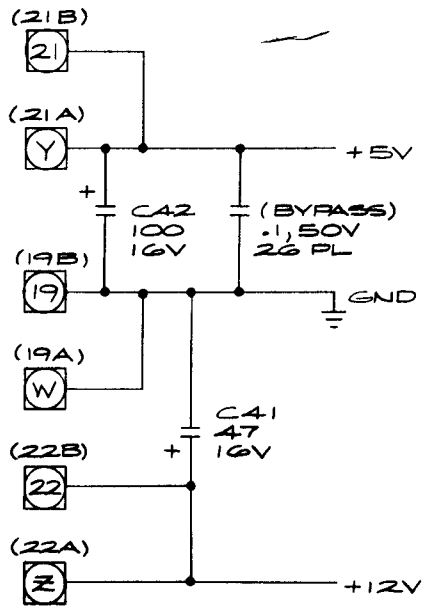
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# Block Diagram (CPU PCB)



# CPU Power Input



## NOTES:

1.  = CONNECTOR CN2
2.  = CONNECTOR CN1



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## Kangaroo CPU PCB Schematic Diagram

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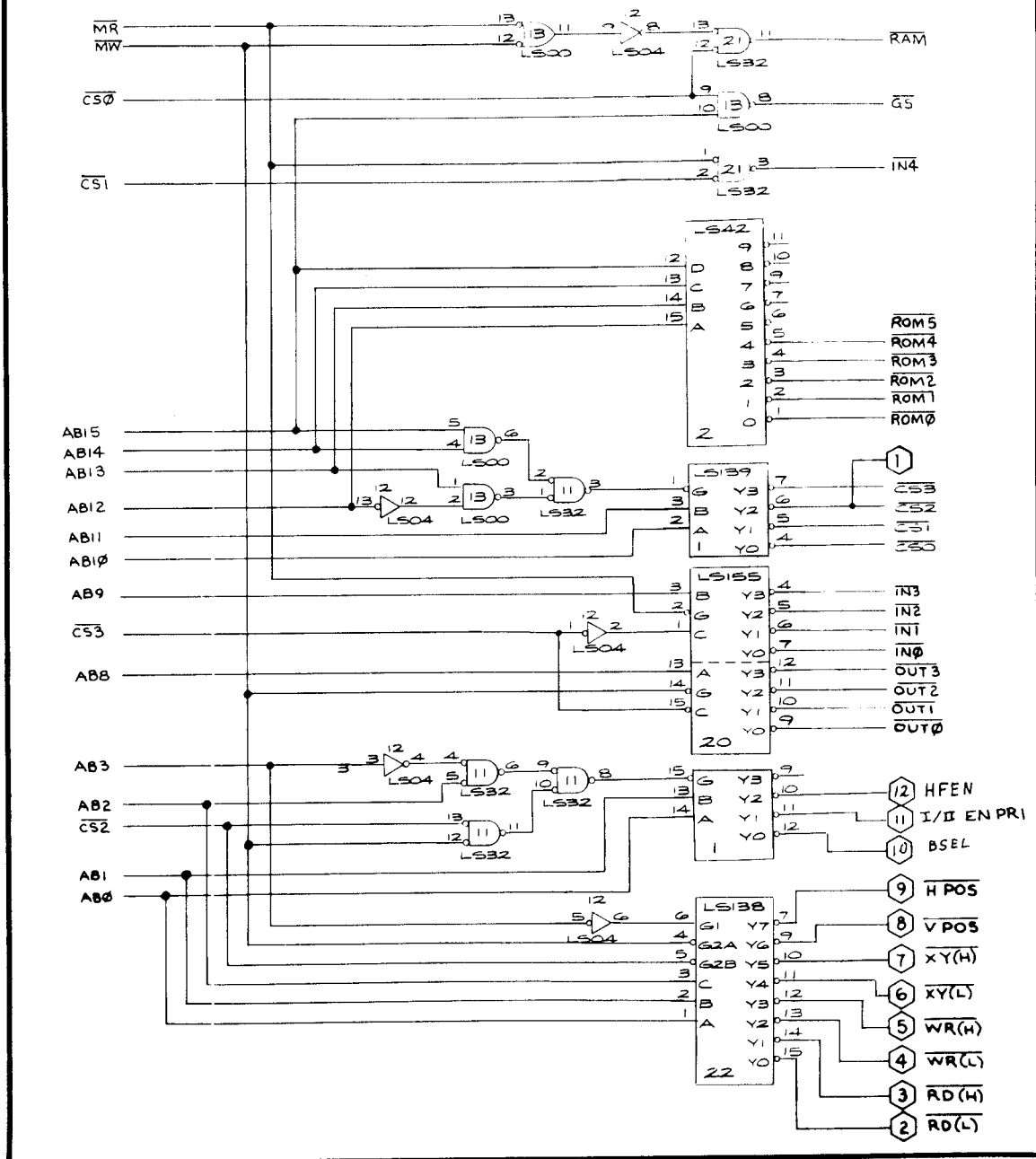
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# Memory Map

| HEXA-DECIMAL ADDRESS                            | R/W | DATA<br>D7 D6 D5 D4 D3 D2 D1 D0 |   |   |   |   |   |   |   | FUNCTION   |
|---|-----|---------------------------------|---|---|---|---|---|---|---|--|
| <b>Game Microprocessor Memory Space (IC15)</b>  |     |                                 |   |   |   |   |   |   |   |  |
| 0000-5FFF                                       | R   | D                               | D | D | D | D | D | D | D | Z80 24K Program ROM  |
| E000-E3FF                                       | R/W | D                               | D | D | D | D | D | D | D | 1K Working RAM   |
| E400  | R   | D                               | D | D | D | D | D | D | D | Option Switch  |
| E800  | W   | D                               | D | D | D | D | D | D | D | Low Byte } Start Address of Data in Picture<br>High Byte } ROM for DMA                             |
| E801  | W   | D                               | D | D | D | D | D | D | D |  |
| E802  | W   | D                               | D | D | D | D | D | D | D | Low Byte } Start Address in Bit Map RAM (where<br>High Byte } picture is to be written) During DMA |
| E803  | W   | D                               | D | D | D | D | D | D | D |  |
| E804  | W   | D                               | D | D | D | D | D | D | D | Low Byte } Picture Size for DMA<br>High Byte } and DMA Start                                       |
| E805  | W   | D                               | D | D | D | D | D | D | D |  |
| E806  | W   | D                               | D | D | D | D | D | D | D | Vertical Start Address in Bit Map  |
| E807  | W   | D                               | D | D | D | D | D | D | D | Horizontal Start Address in Bit Map  |
| E808  | W   |                                 |   |   |   |   |   | D | D | Bank Select Latch  |
| E809  | W   |                                 |   |   | D | D | D | D | D | A & B Bit Map Control Latch (A = playfield, B = motion)  |
| E80A  |     |                                 |   |   | D | D | D | D | D | Color-Shading Latch  |
| EC00  | W   | D                               | D | D | D | D | D | D | D | Sound DATA to Sound Microprocessor   |
| EC00  | R   |                                 |   |   |   |   |   |   | D | Utility Coin Switch  |
| EC00  | R   |                                 |   |   |   |   |   | D |   | 1 Player Start   |
| EC00  | R   |                                 |   |   |   |   | D |   |   | 2 Player Start   |
| EC00  | R   |                                 |   |   |   | D |   |   |   | Left Coin Input  |
| EC00  | R   |                                 |   |   | D |   |   |   |   | Right Coin Input   |
| ED00  | W   |                                 |   |   |   |   |   |   | D | Coin Counter 1   |
| ED00  | W   |                                 |   |   |   |   |   |   | D | Coin Counter 2 (European games)  |
| ED00  | R   |                                 |   |   |   |   |   |   | D | Player 1 Right   |
| ED00  | R   |                                 |   |   |   |   |   |   | D | Player 1 Left  |
| ED00  | R   |                                 |   |   |   |   | D |   |   | Player 1 Up  |
| ED00  | R   |                                 |   |   |   | D |   |   |   | Player 1 Down  |
| ED00  | R   |                                 |   |   | D |   |   |   |   | Player 1 Punch   |
| EE00  | R   |                                 |   |   |   |   |   |   | D | Player 2 Right   |
| EE00  | R   |                                 |   |   |   |   |   |   | D | Player 2 Left  |
| EE00  | R   |                                 |   |   |   |   | D |   |   | Player 2 Up  |
| EE00  | R   |                                 |   |   |   | D |   |   |   | Player 2 Down  |
| EE00  | R   |                                 |   |   | D |   |   |   |   | Player 2 Punch   |
| EFXX  | W   |                                 |   |   |   | D | D | D | D | Output to Custom Microcomputer   |
| EFXX  | R   |                                 |   |   |   | D | D | D | D | Input from Custom Microcomputer  |
| <b>Sound Microprocessor Memory Space (IC34)</b> |     |                                 |   |   |   |   |   |   |   |  |
| 0000-0FFF                                       | R   | D                               | D | D | D | D | D | D | D | 4K Program ROM   |
| 4000-43FF                                       | R/W | D                               | D | D | D | D | D | D | D | 1K Working RAM   |
| 6000  | R   | D                               | D | D | D | D | D | D | D | Read DATA from Game Microprocessor   |
| 7000  | W   | D                               | D | D | D | D | D | D | D | Write to Sound Chip (GI-AY-3-8910)   |
| 8000  | R   | D                               | D | D | D | D | D | D | D | Read from Sound Chip   |



# Address Decoder



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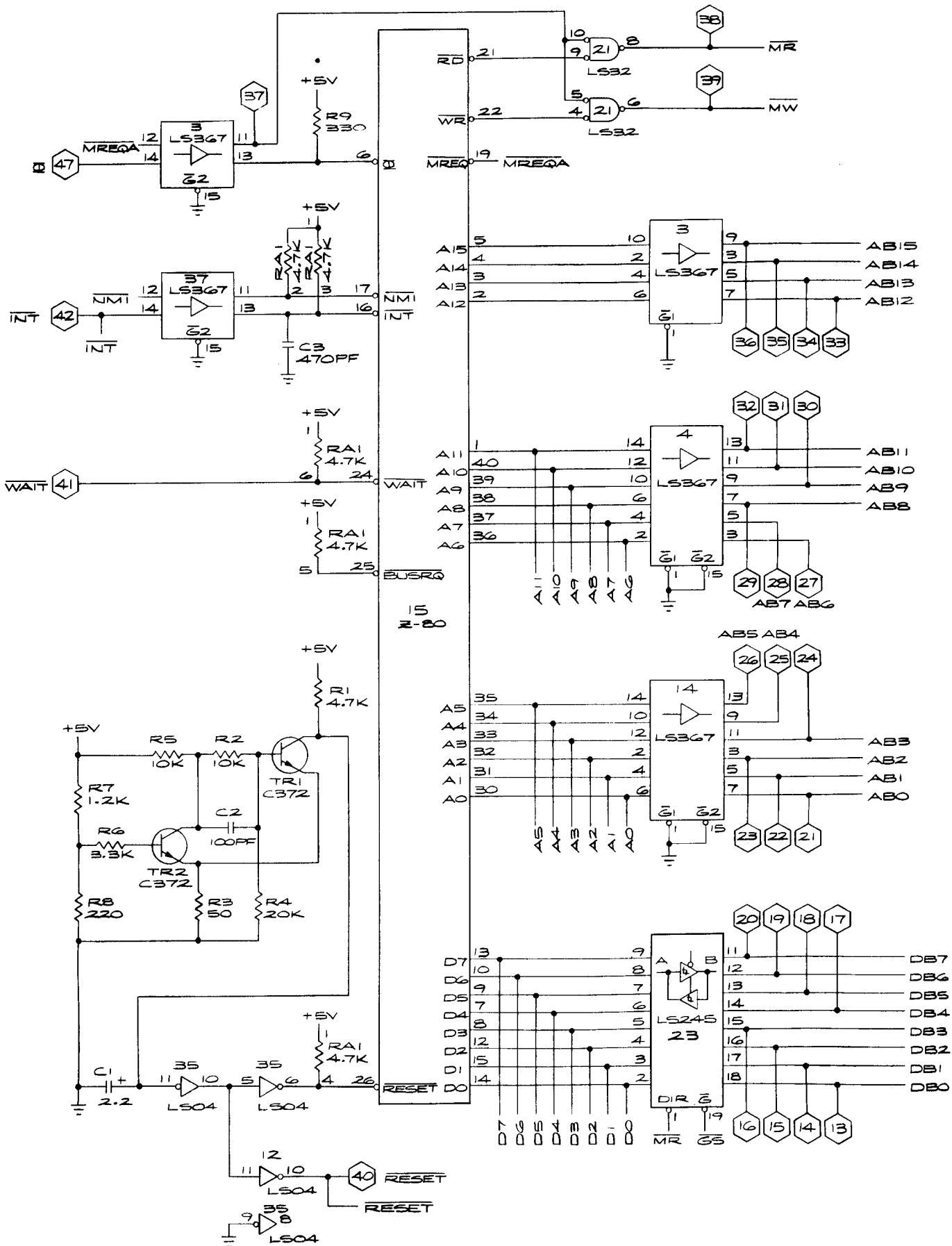
## Kangaroo CPU PCB Schematic Diagram

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# Game Microprocessor





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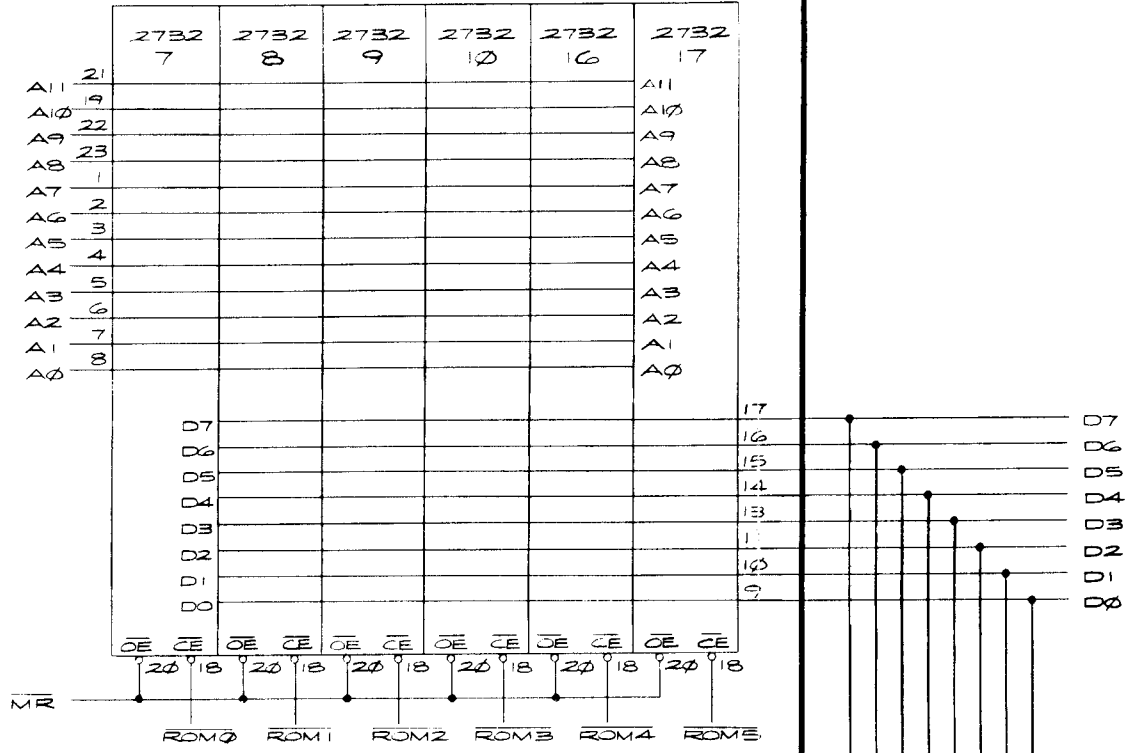
## Kangaroo CPU PCB Schematic Diagram

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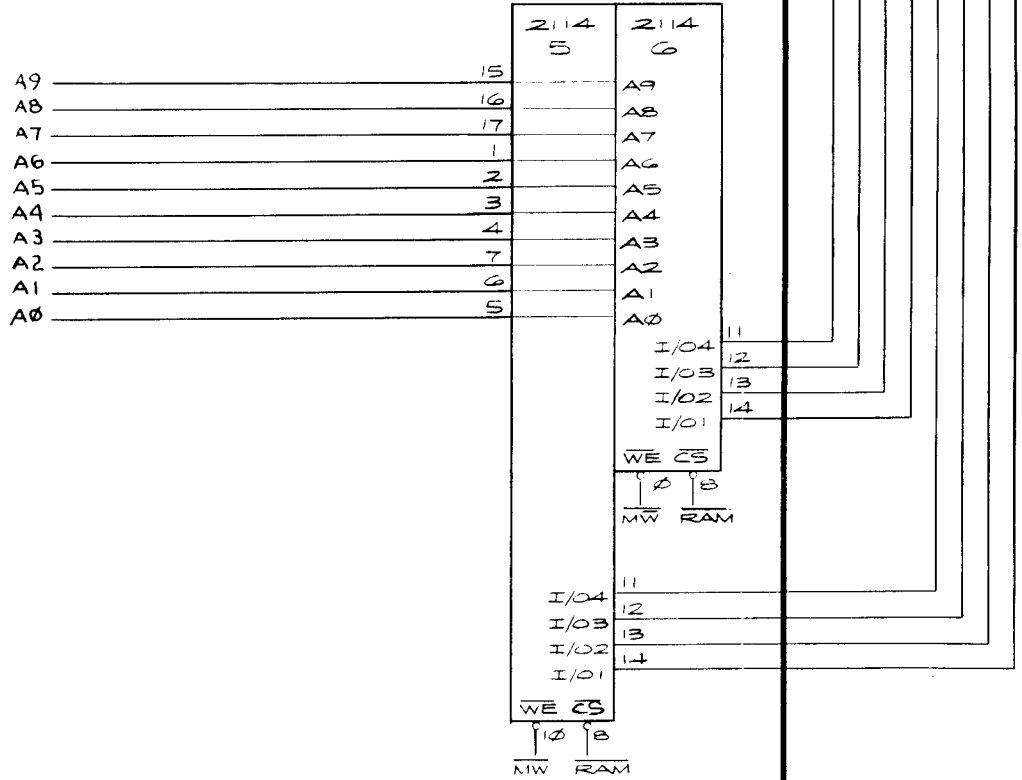
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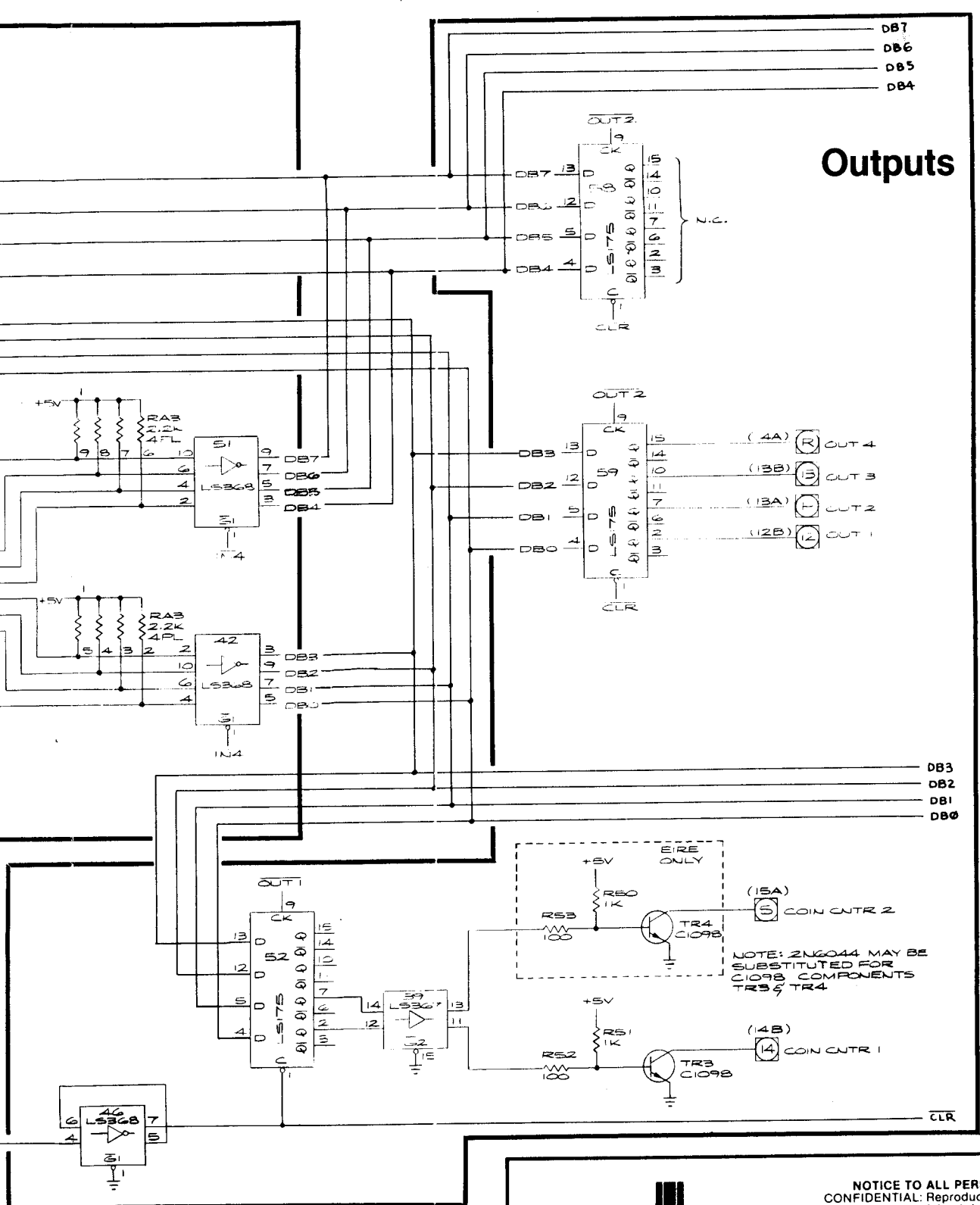
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# Program ROM



# RAM





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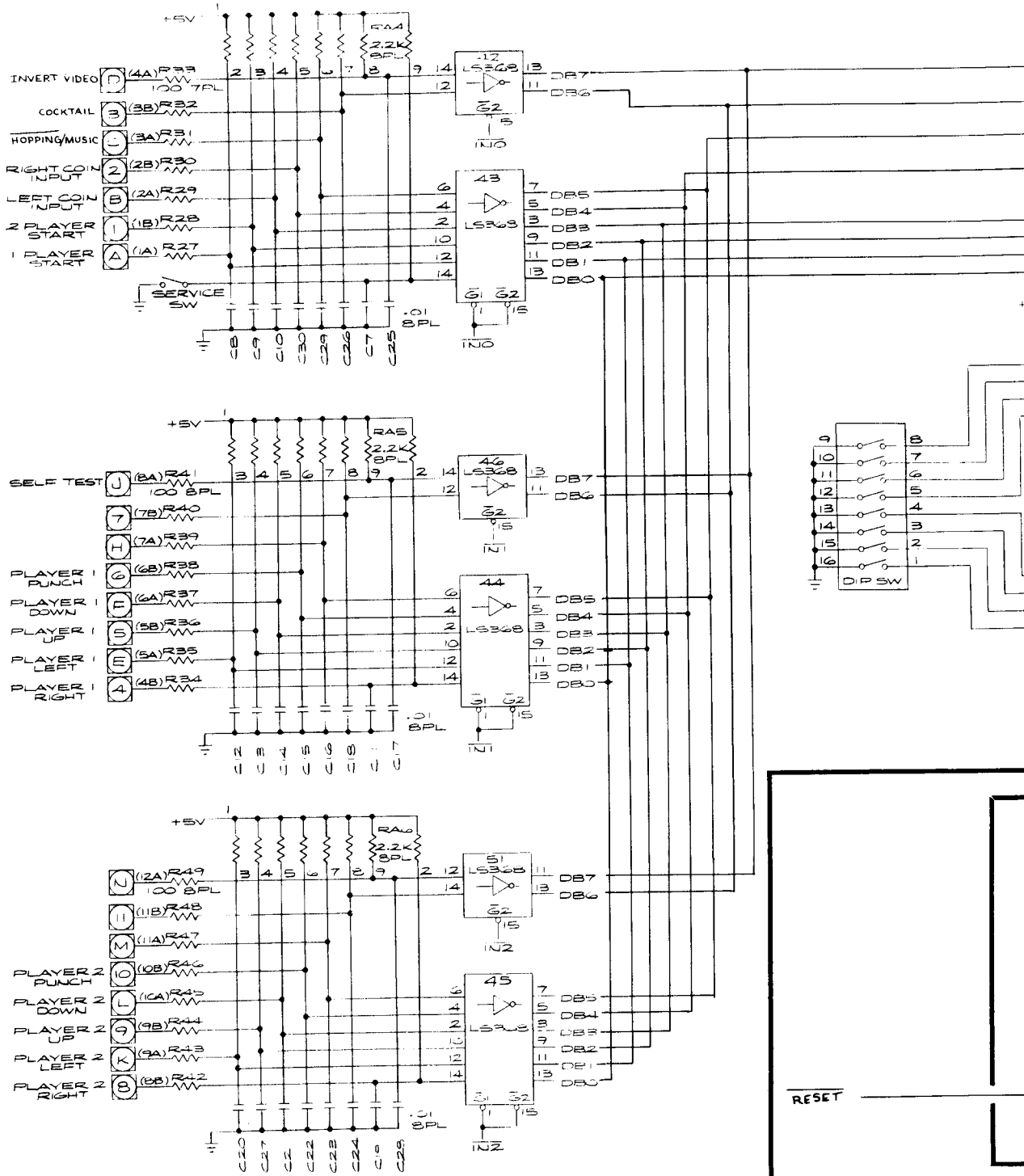
## Kangaroo CPU PCB Schematic Diagram

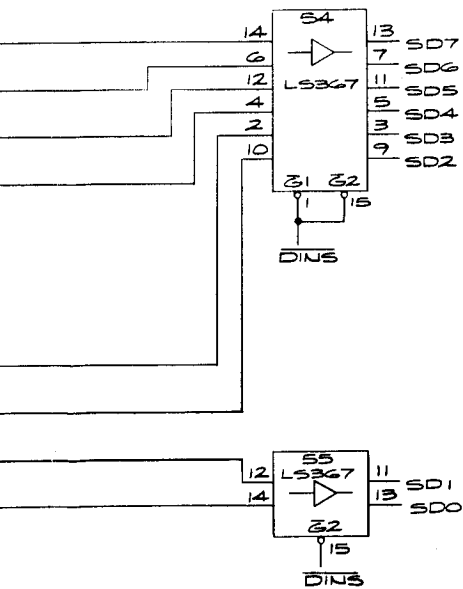
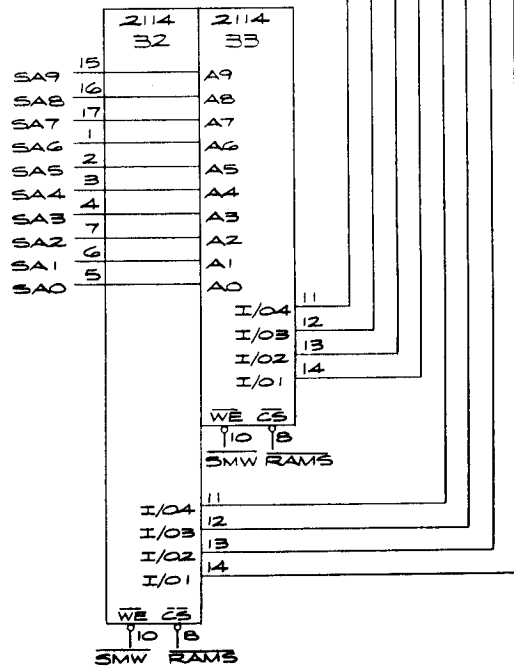
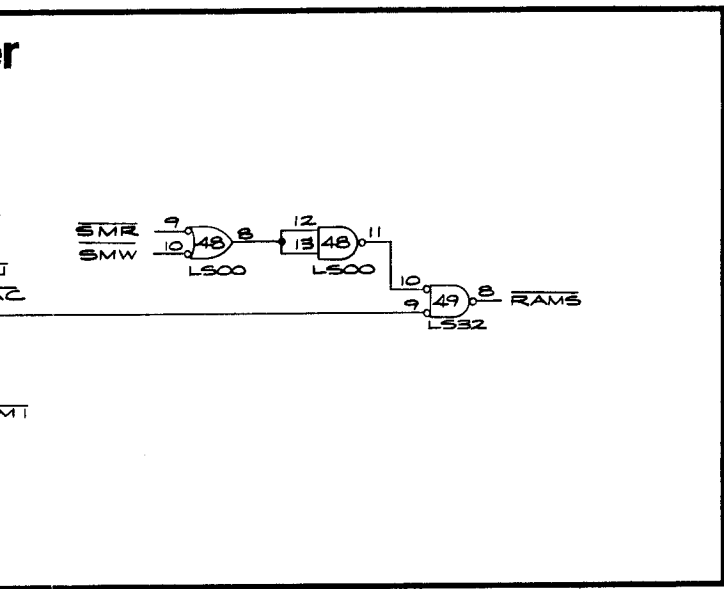
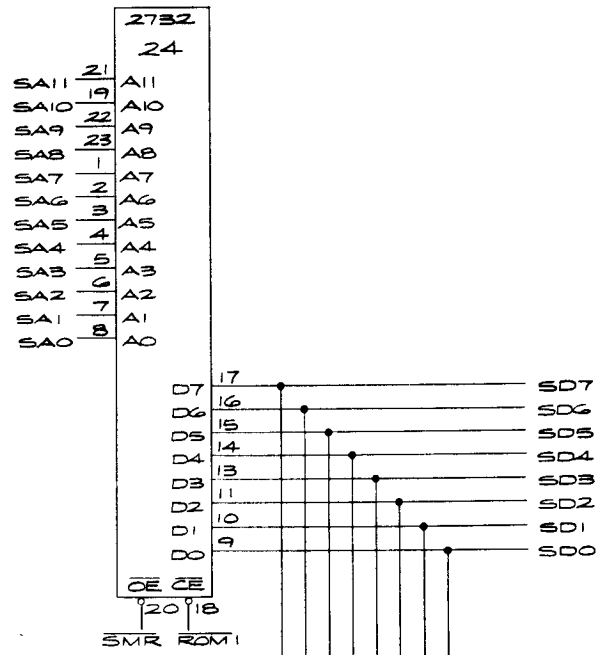
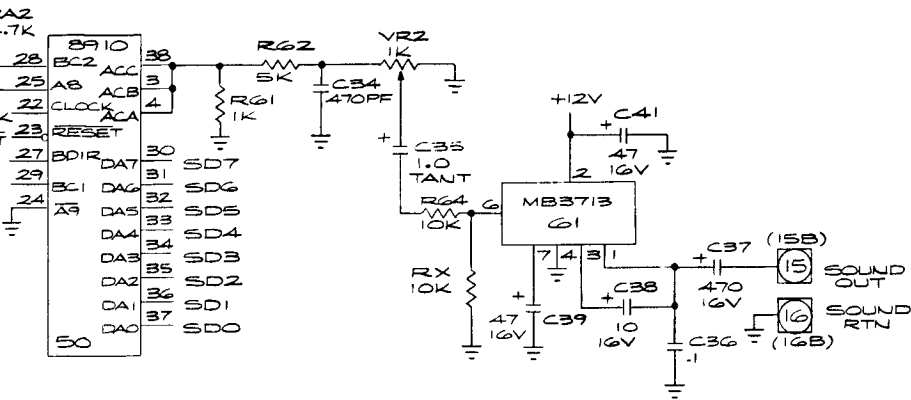
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# Inputs







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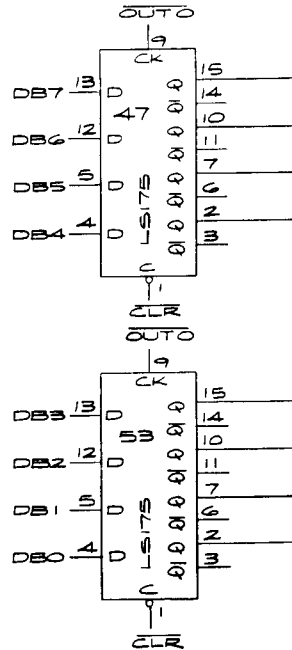
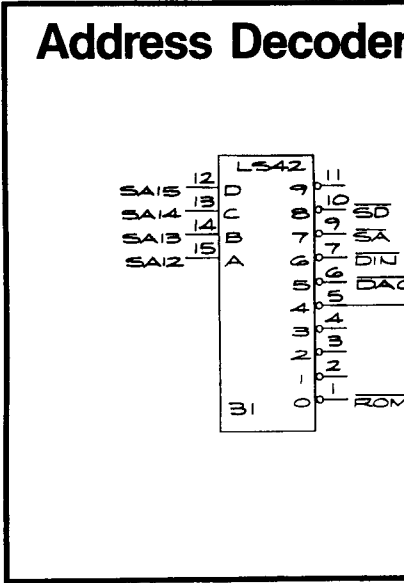
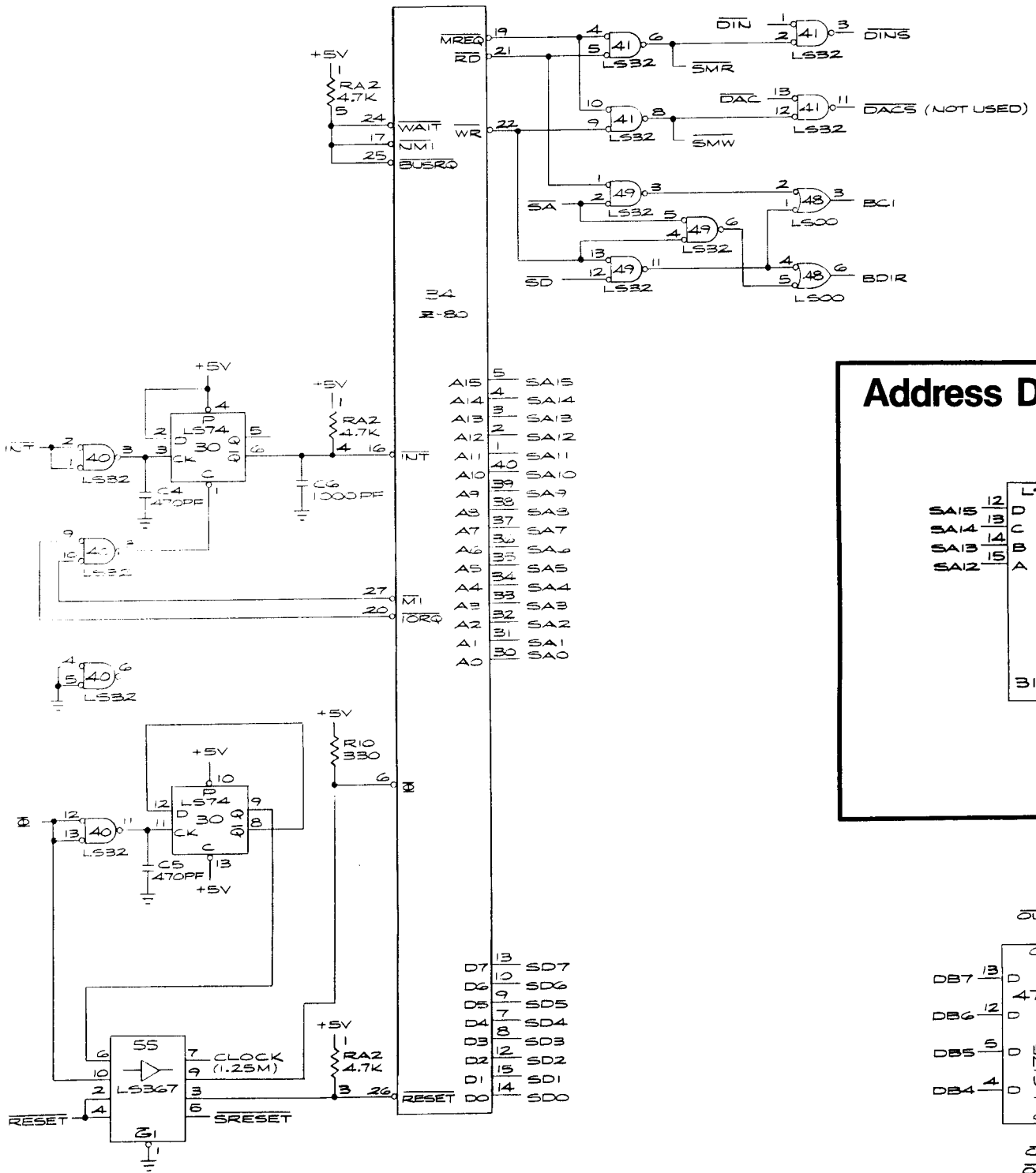
## Kangaroo CPU PCB Schematic Diagram

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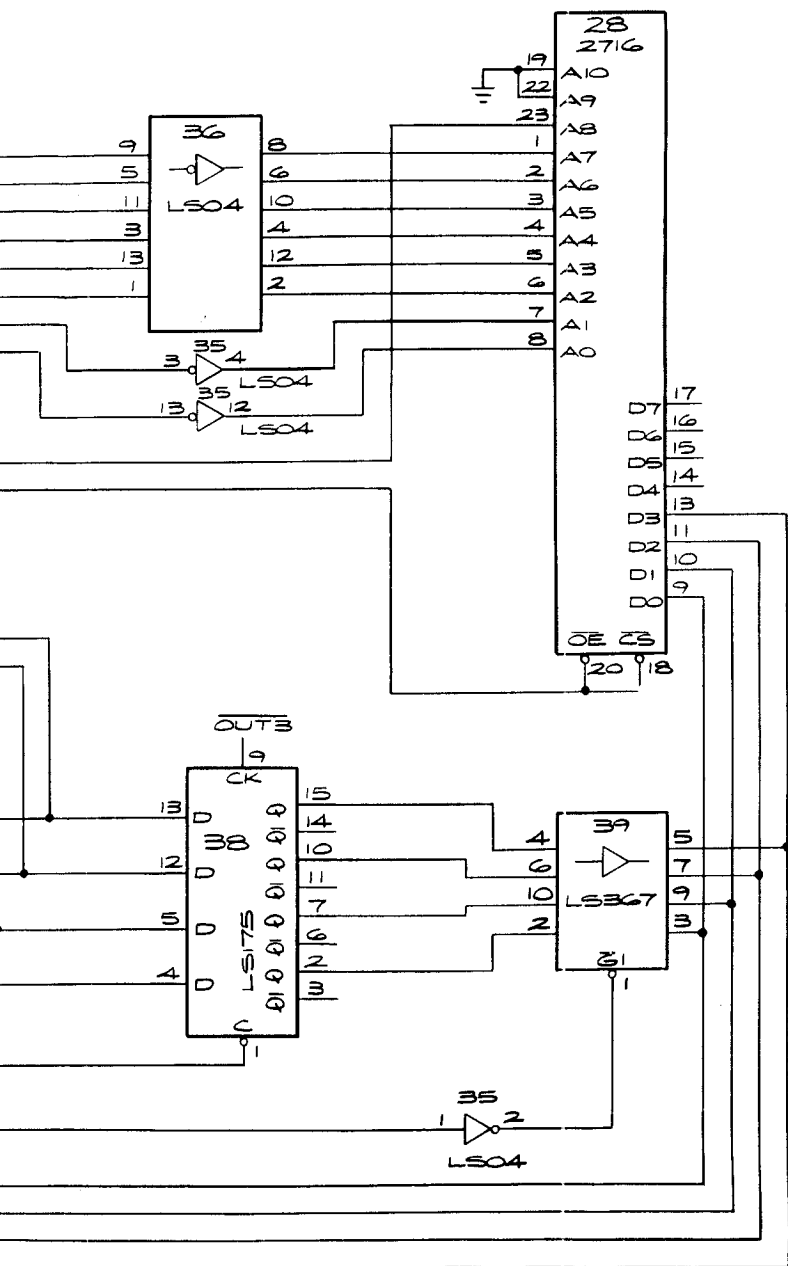
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# Sound Microprocessor







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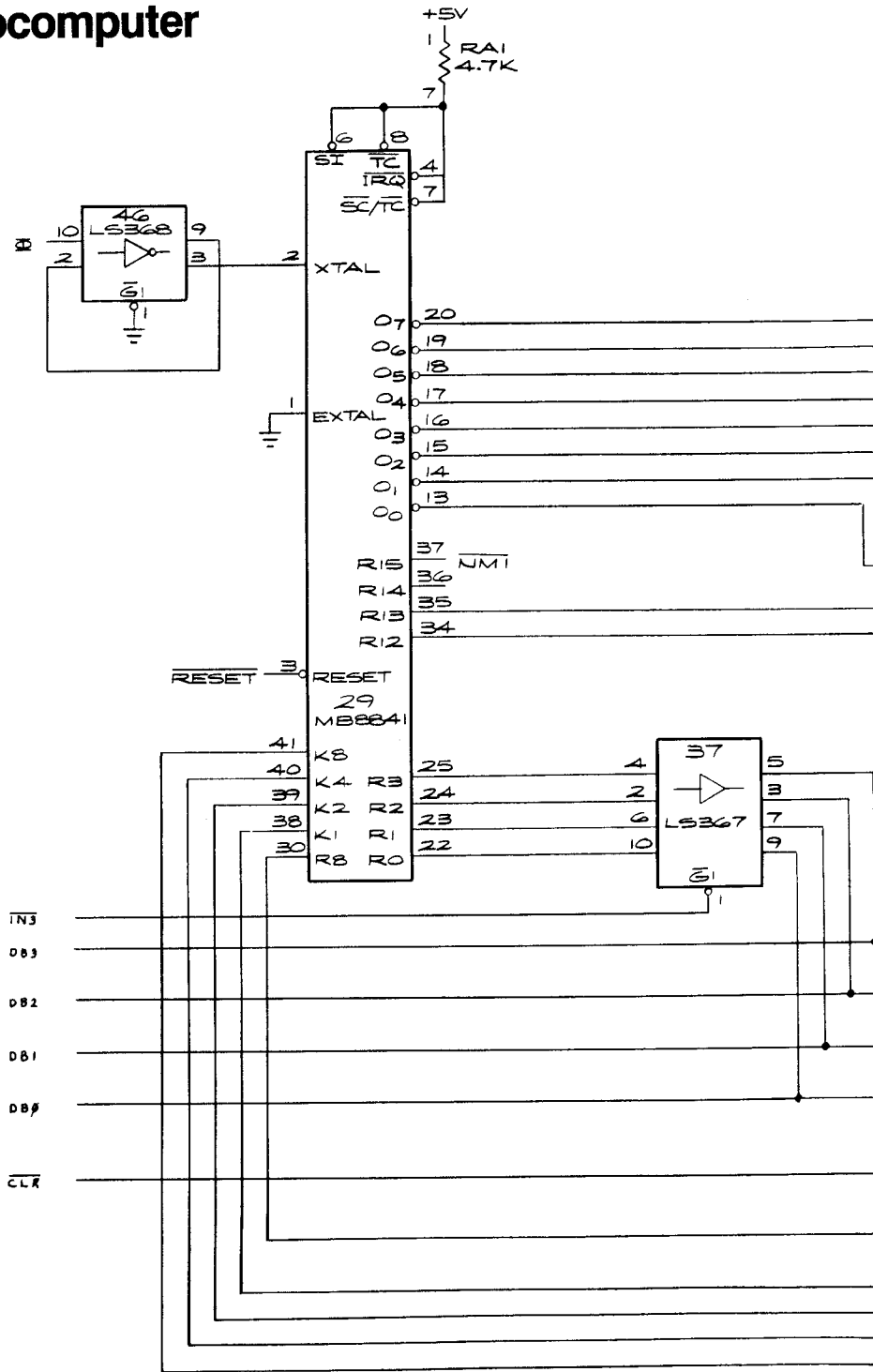
## Kangaroo CPU PCB Schematic Diagram

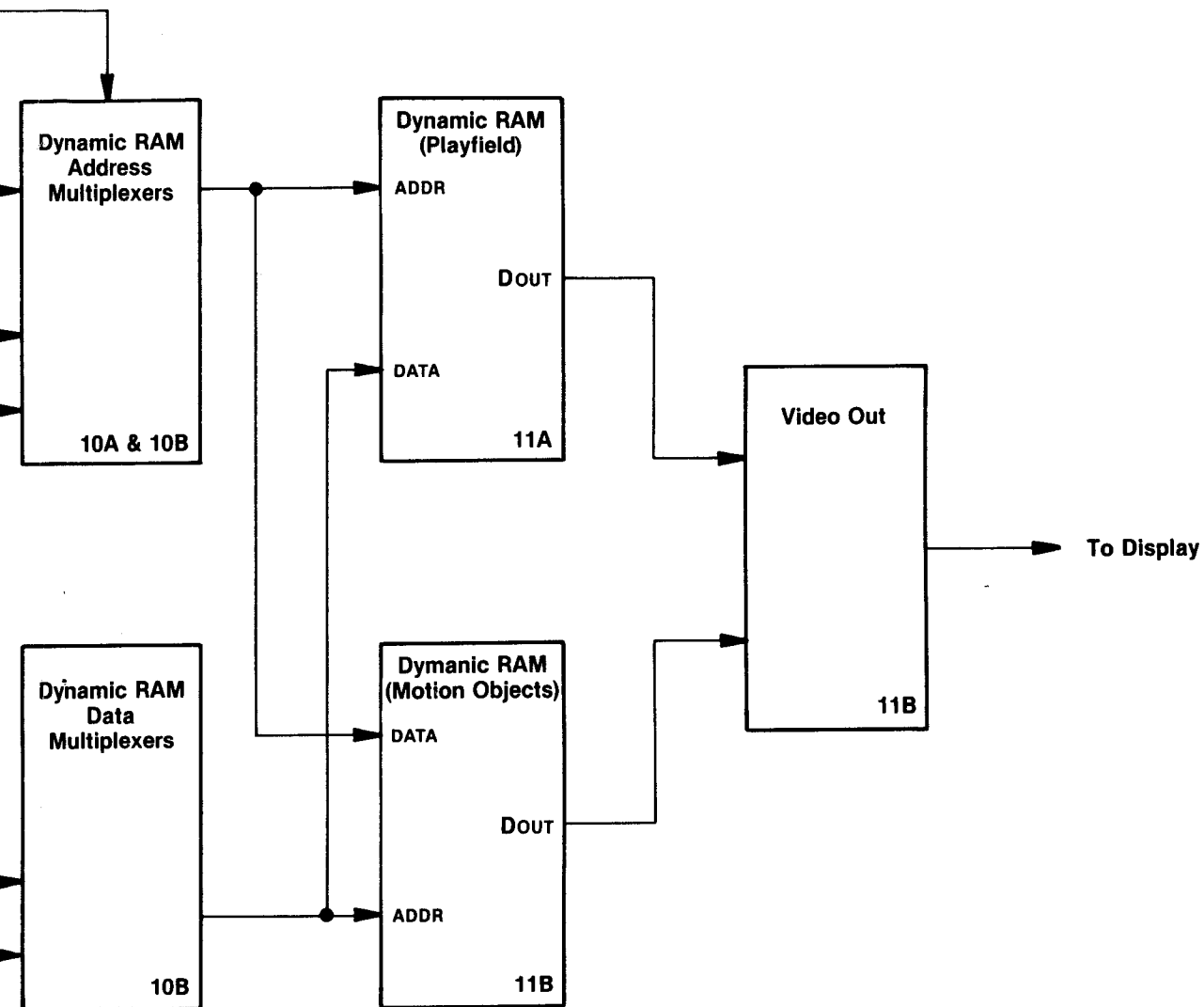
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# Custom Microcomputer





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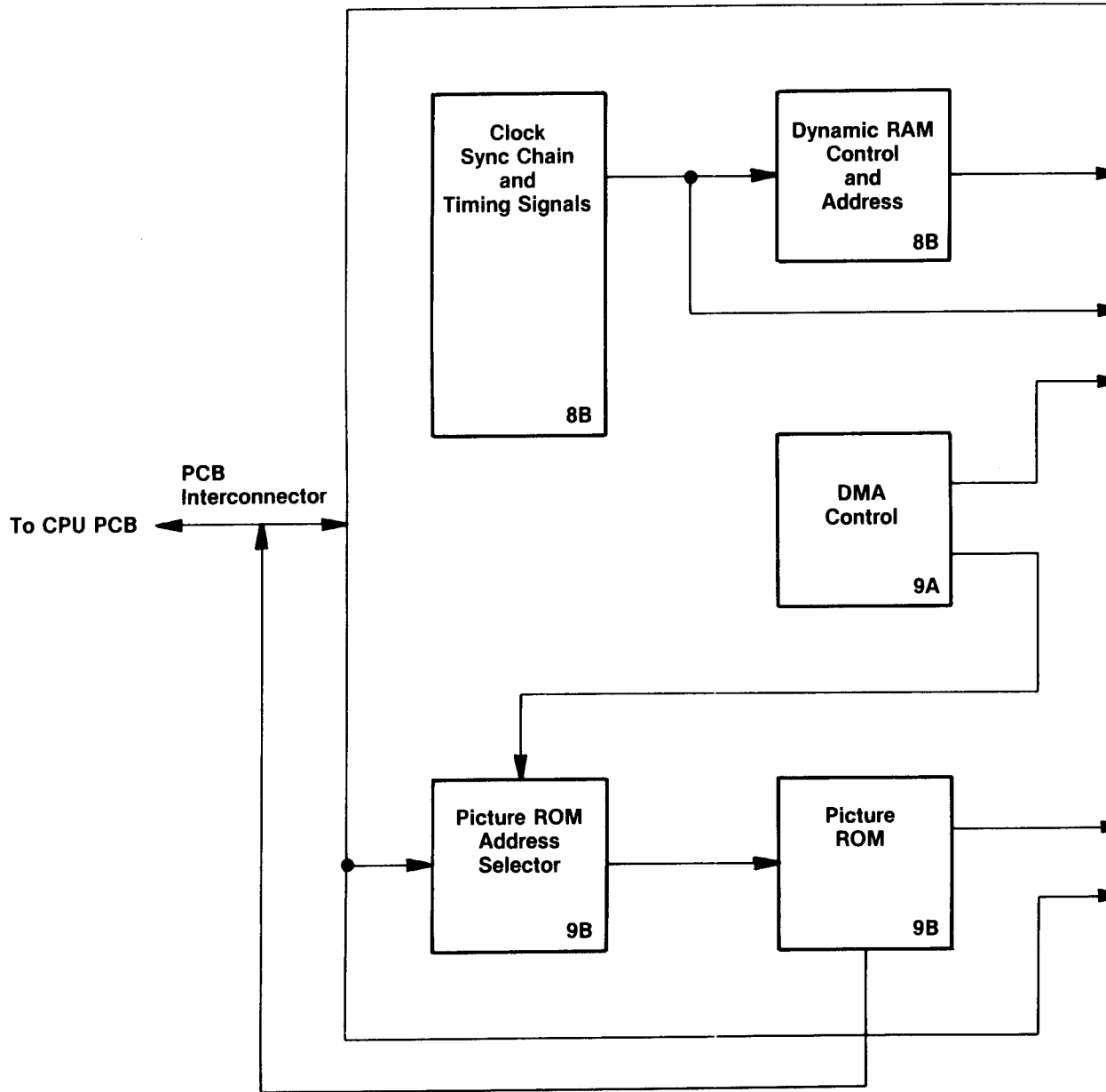
## Kangaroo Video PCB Schematic Diagram

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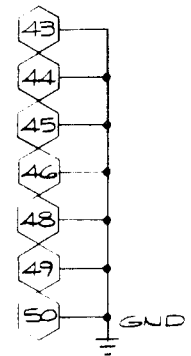
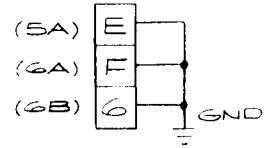
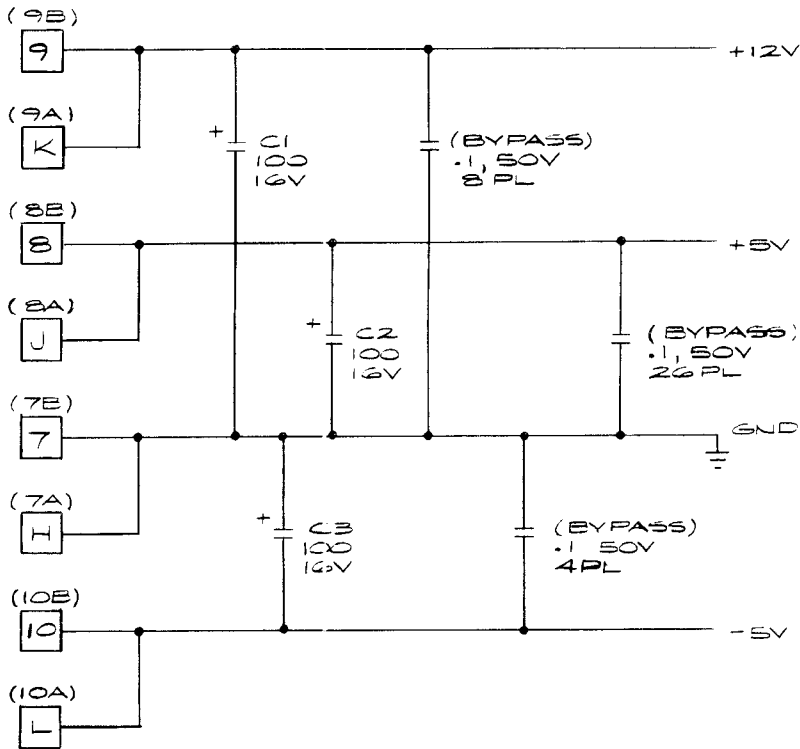
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# Block Diagram (Video PCB)



# Video Power Input



## NOTES:

1.  = CONNECTOR CN1
2.  = CONNECTOR CN4



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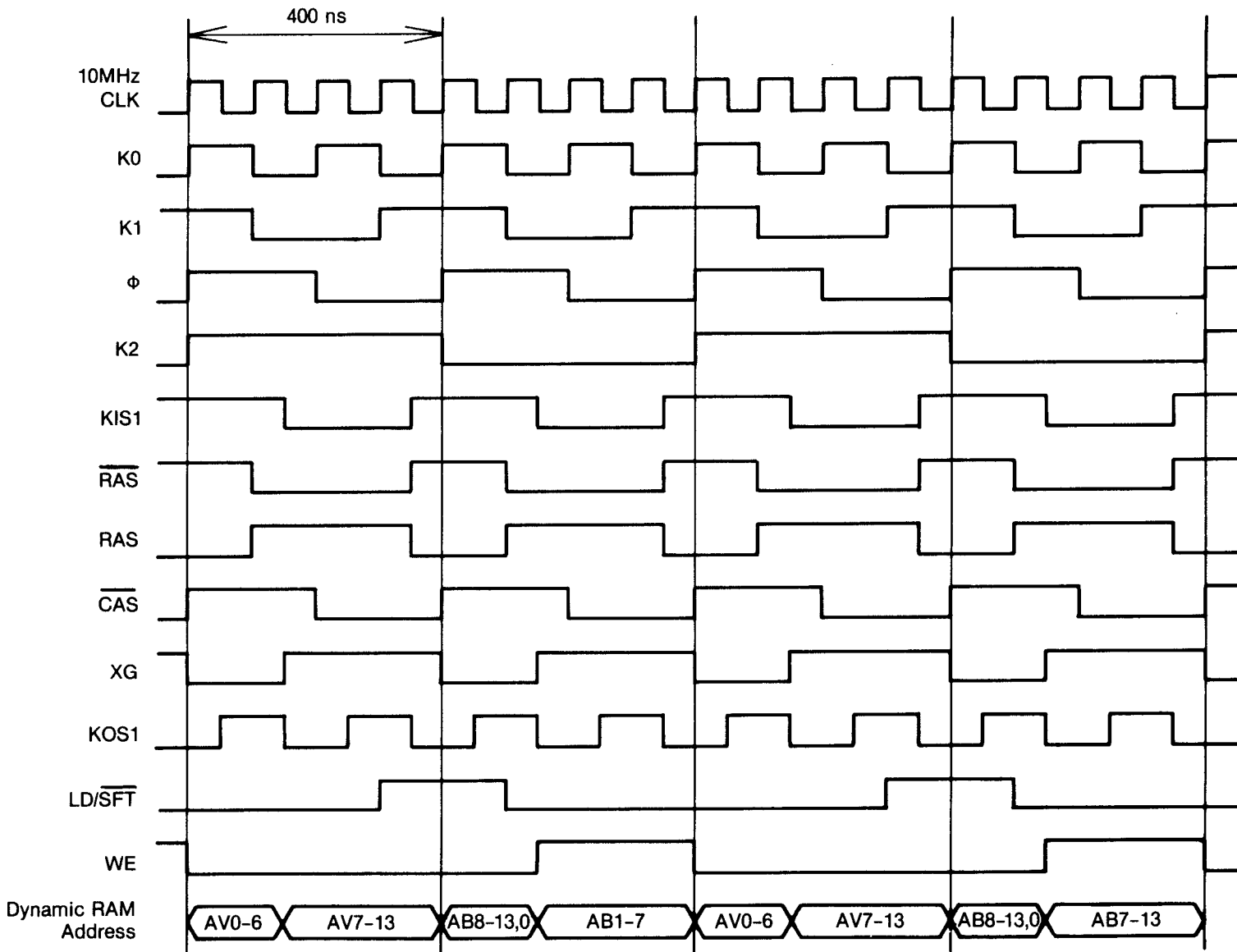
## Kangaroo Video PCB Schematic Diagram

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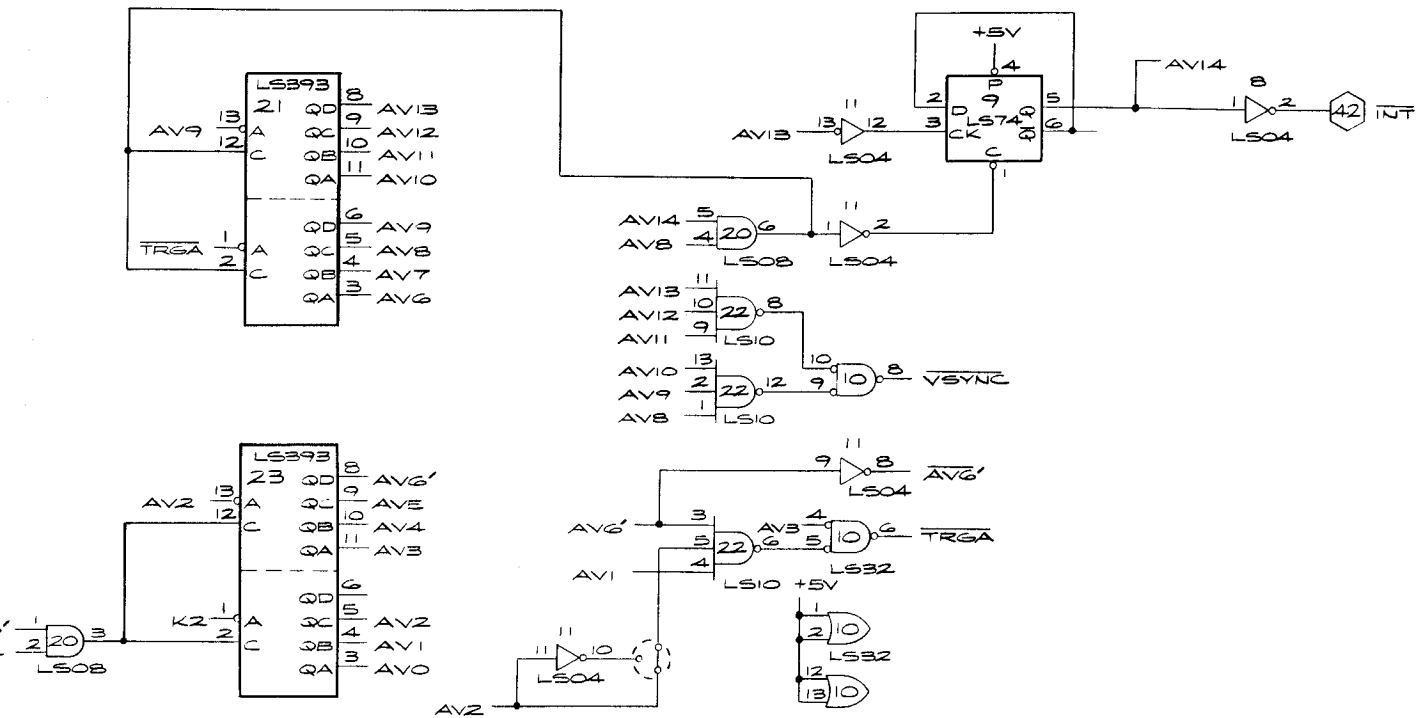
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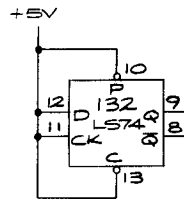
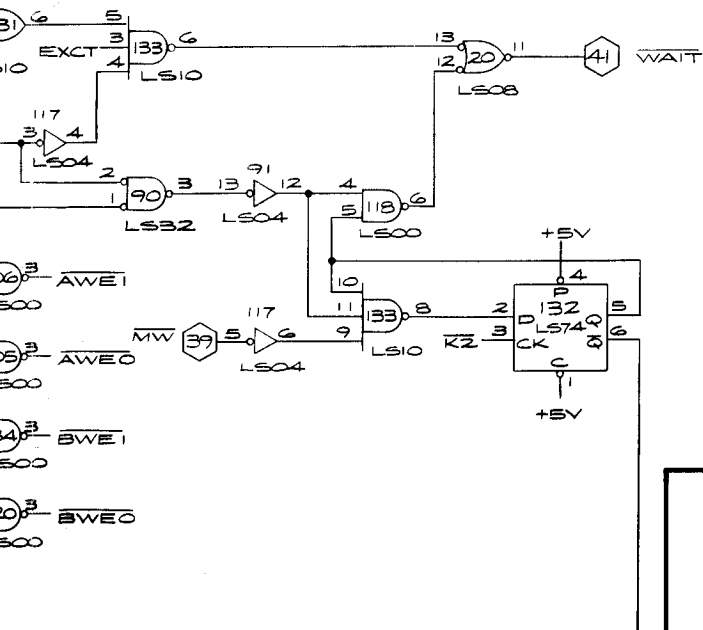
# Dynamic RAM Timing Diagram (Video PCB)



# Timing Signals



# Address Decoding



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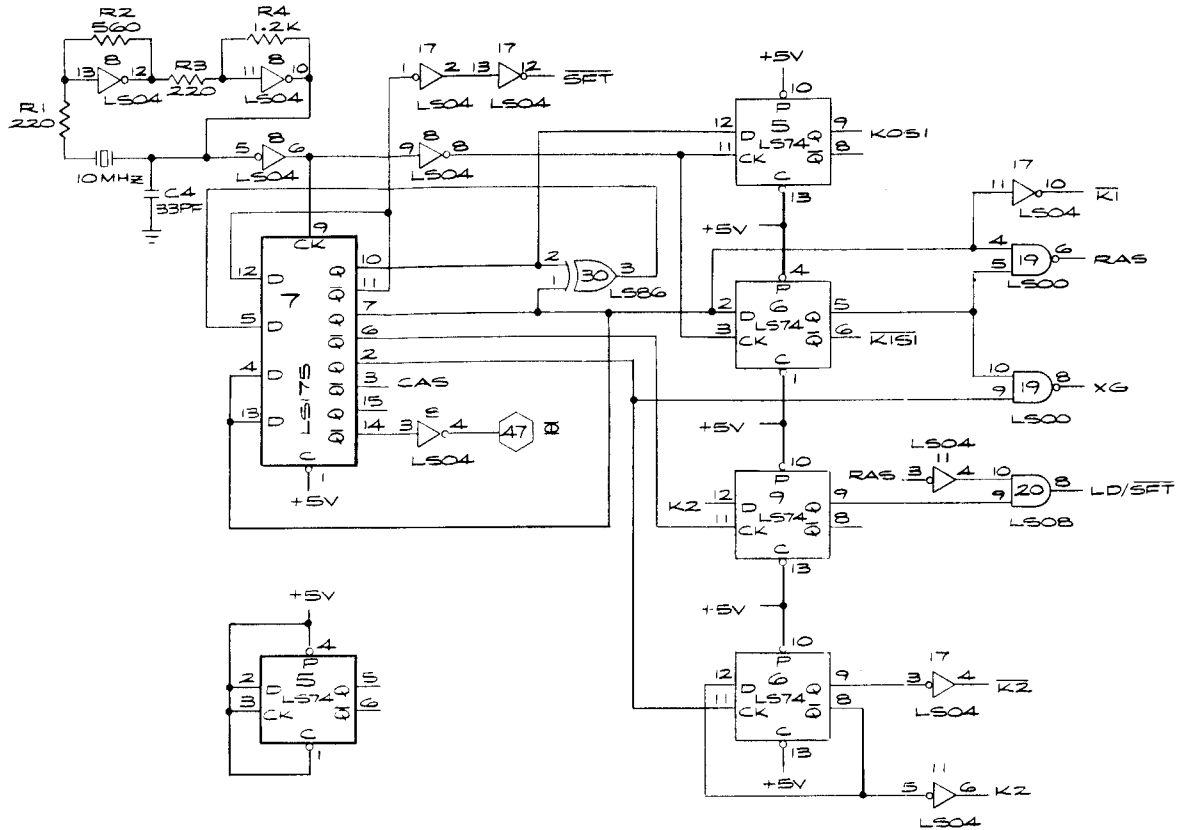
## Kangaroo Video PCB Schematic Diagram

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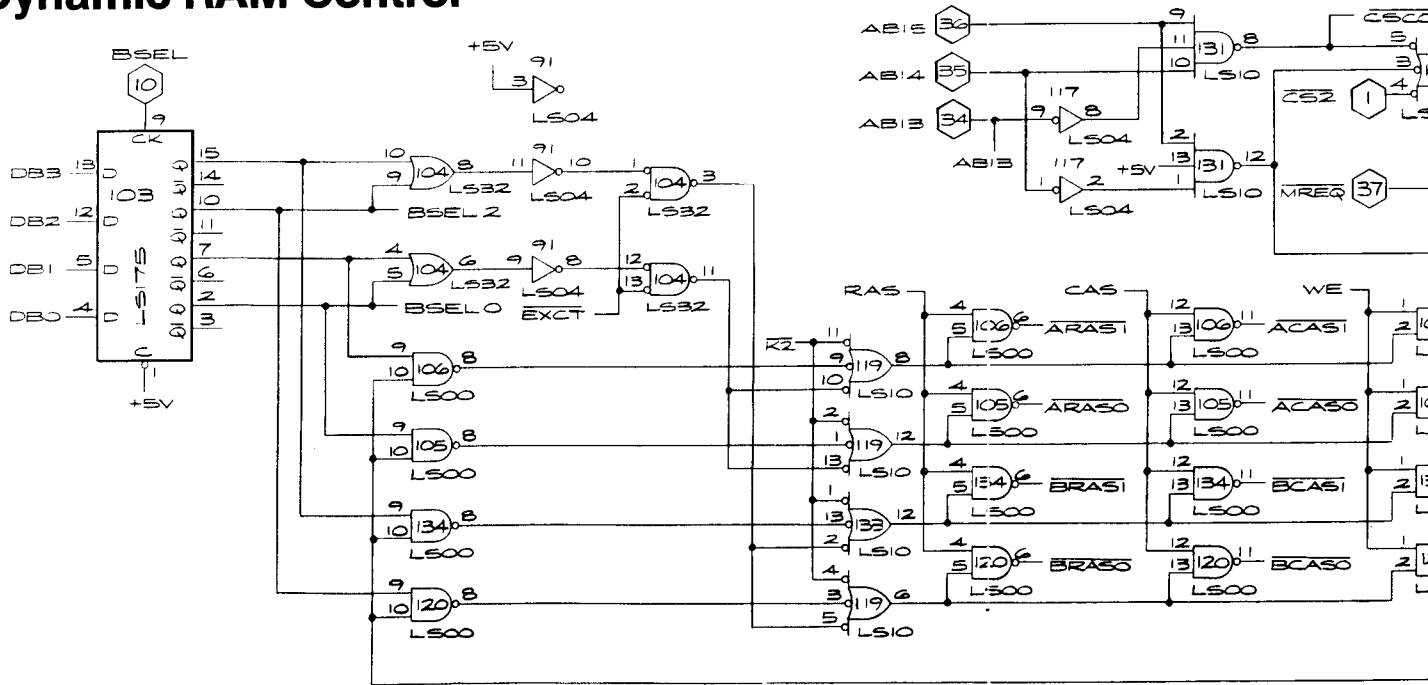
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# Clock, Sync Chain, a

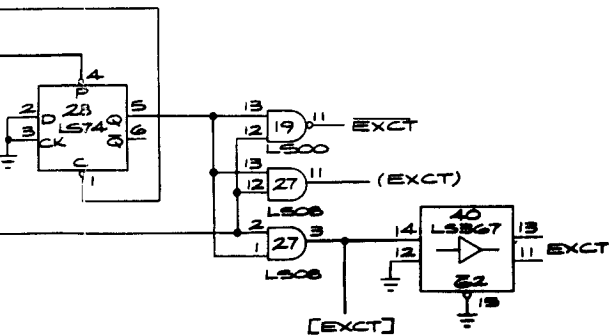
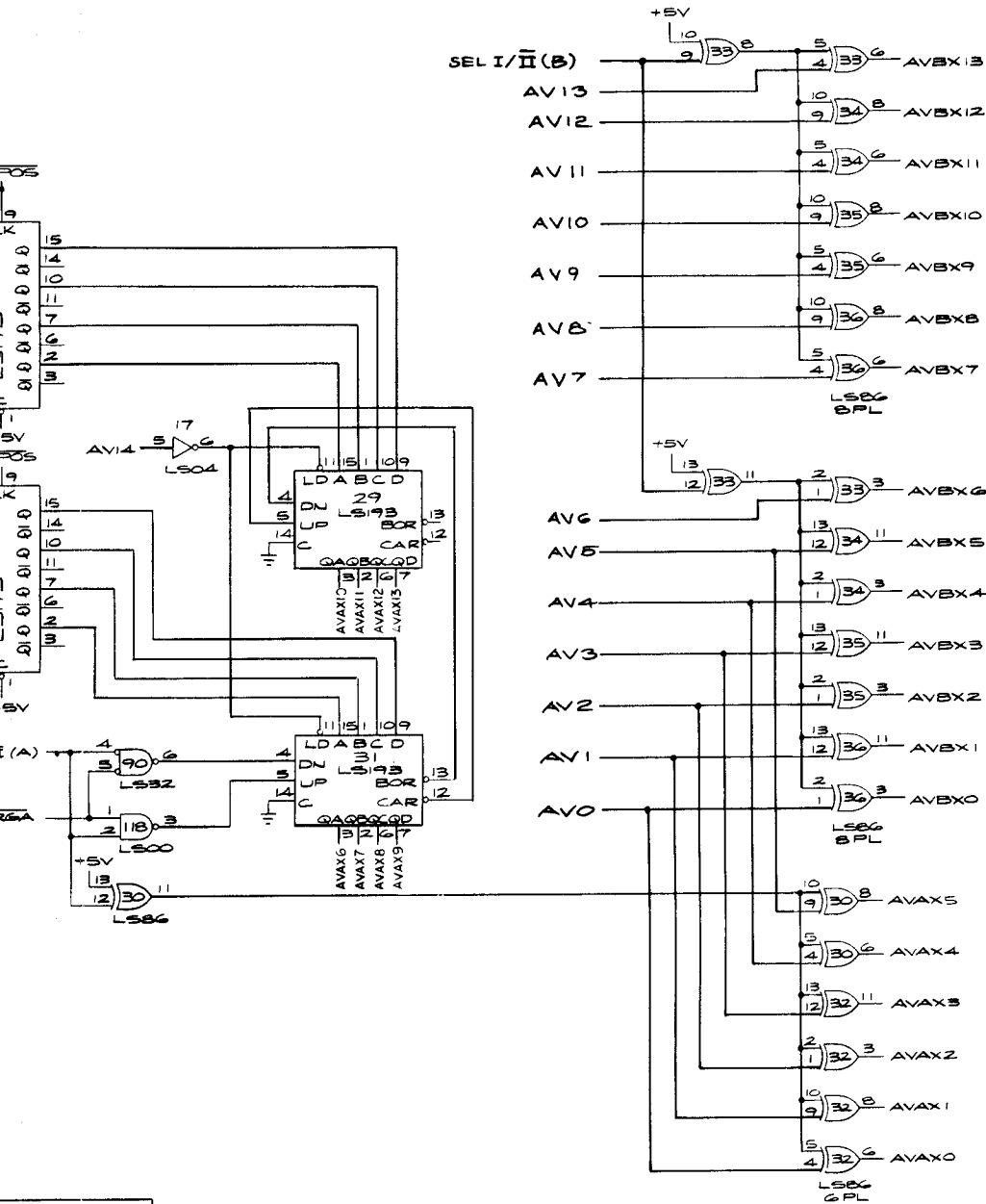


# Dynamic RAM Control





# Dynamic RAM Video Address and Flip



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## Kangaroo Video PCB Schematic Diagram

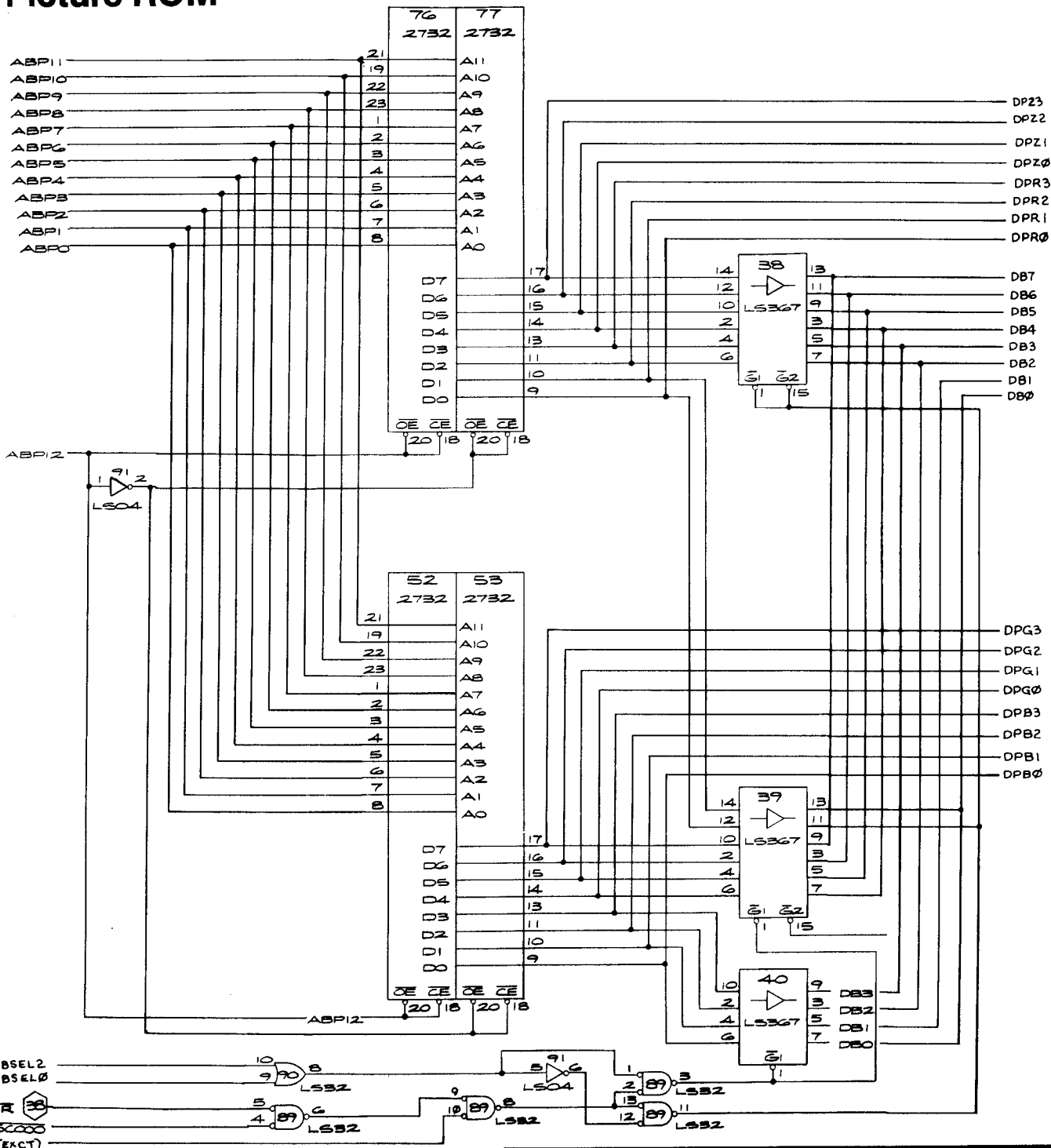
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# Picture ROM



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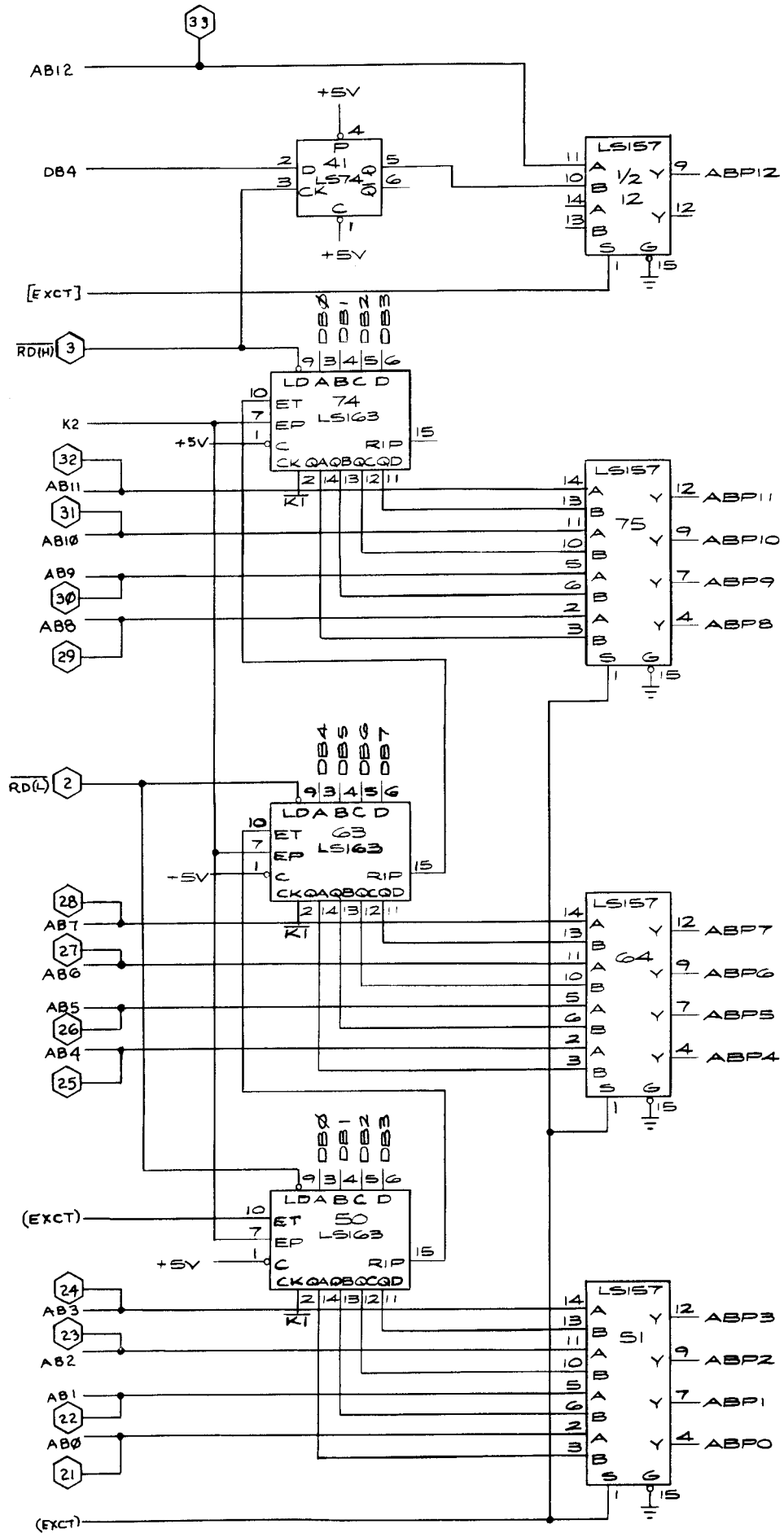
## Kangaroo Video PCB Schematic Diagram

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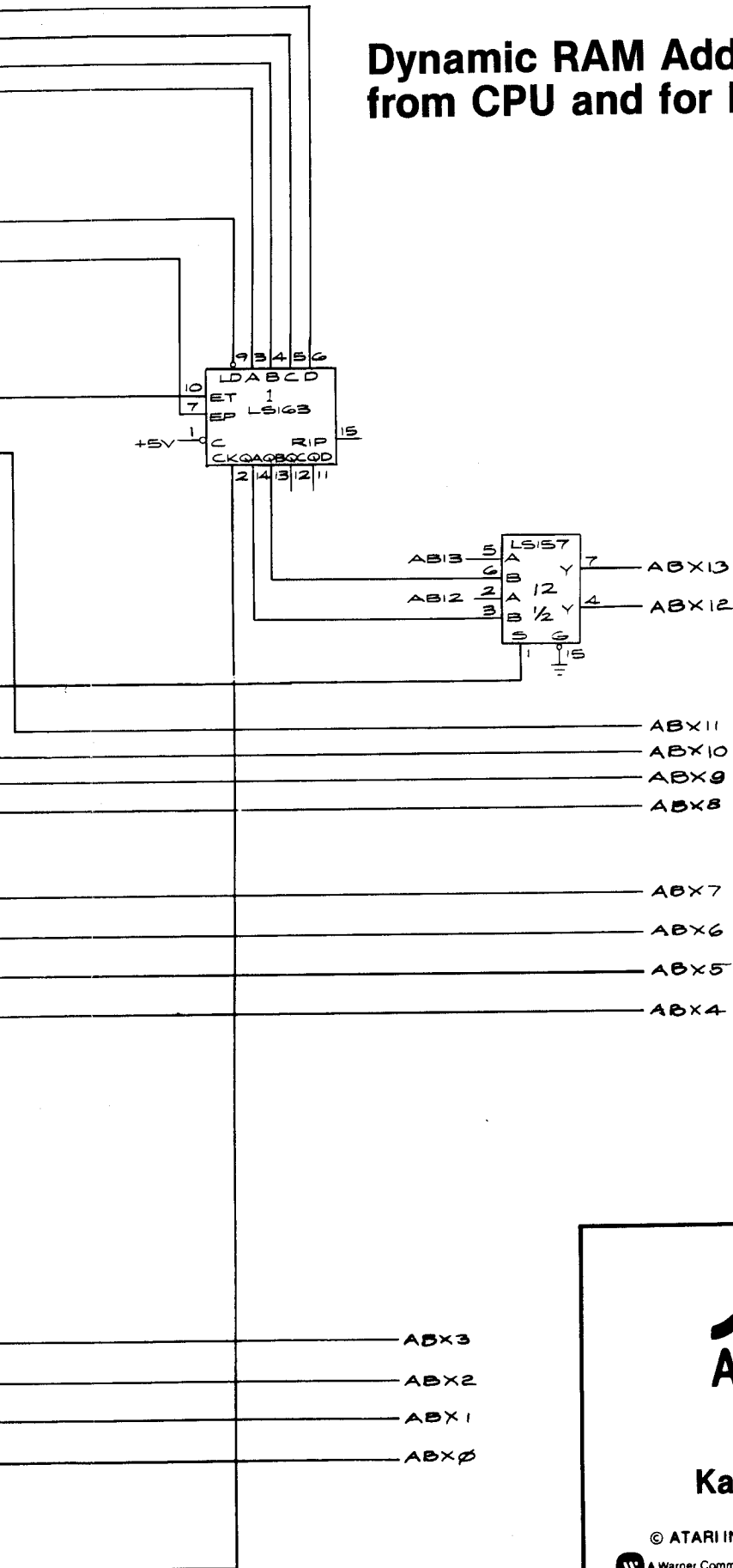
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# Picture ROM Address Selector



# Dynamic RAM Address from CPU and for DMA



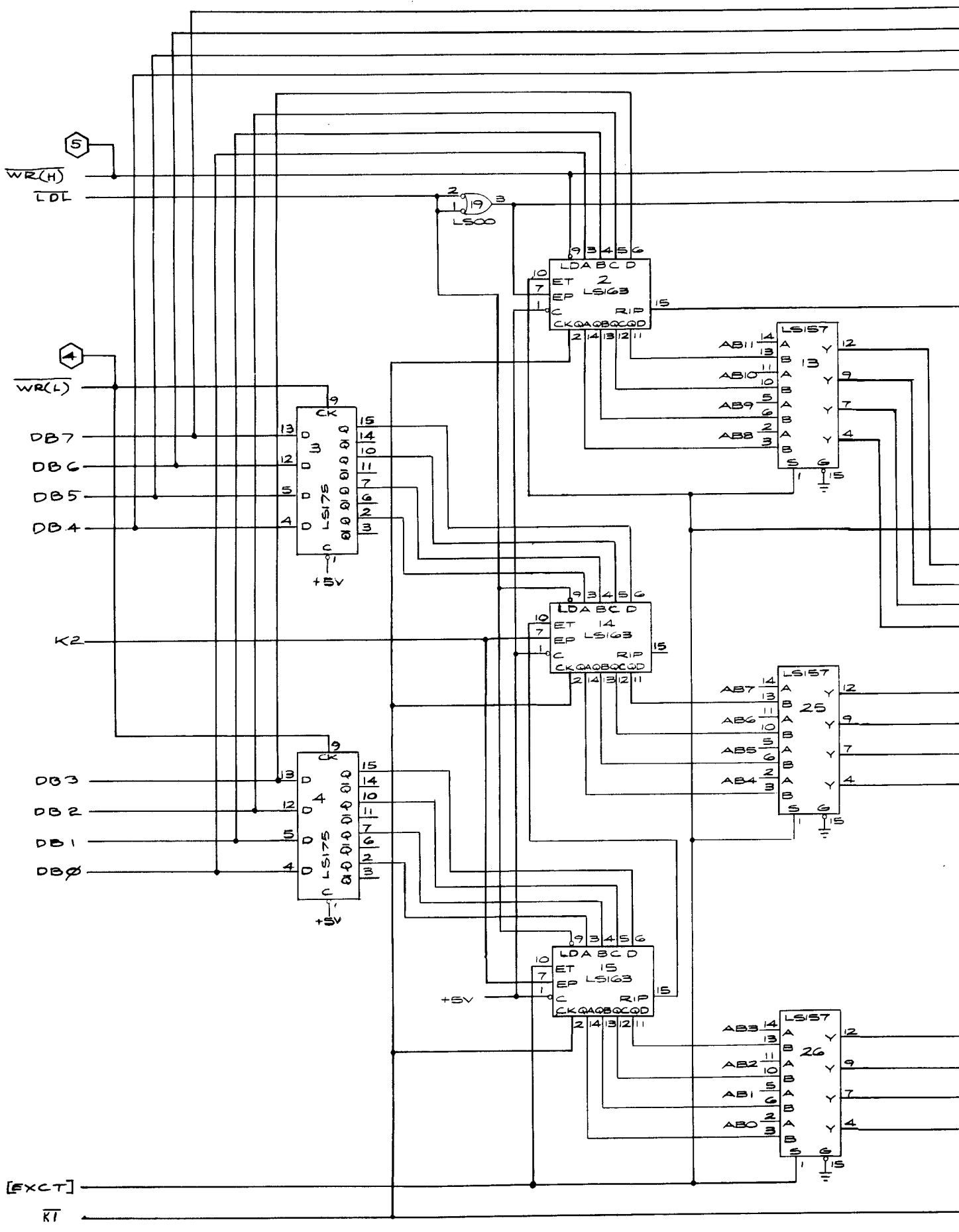
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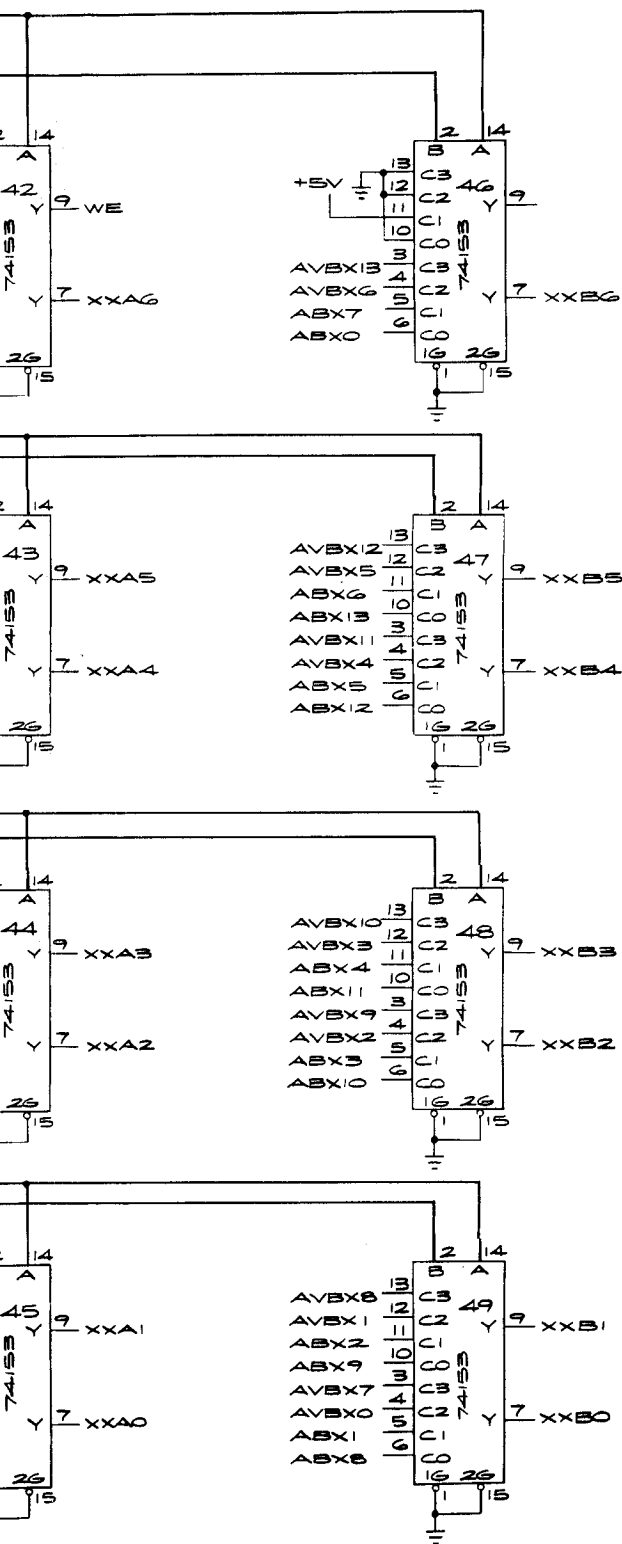
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# Address Selector



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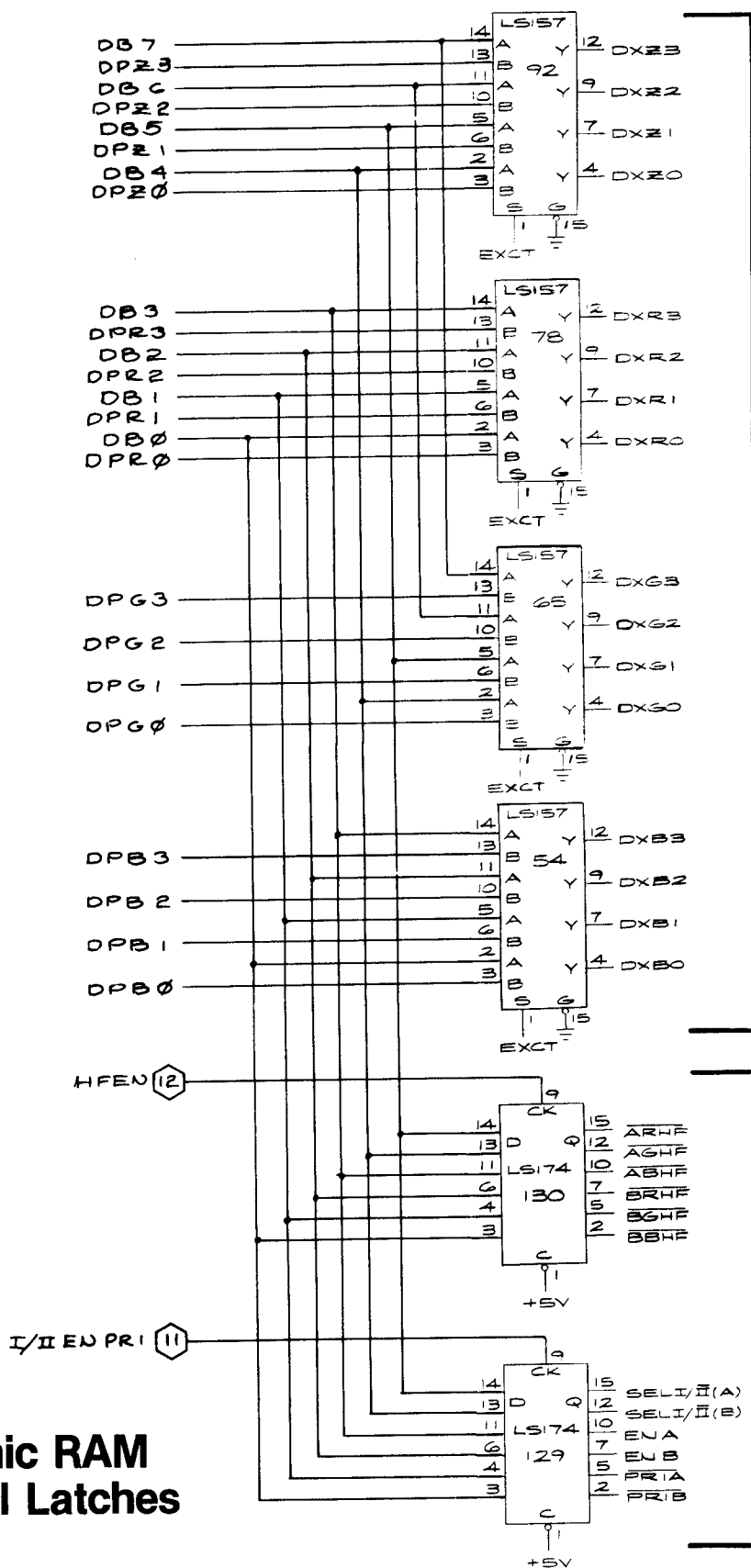
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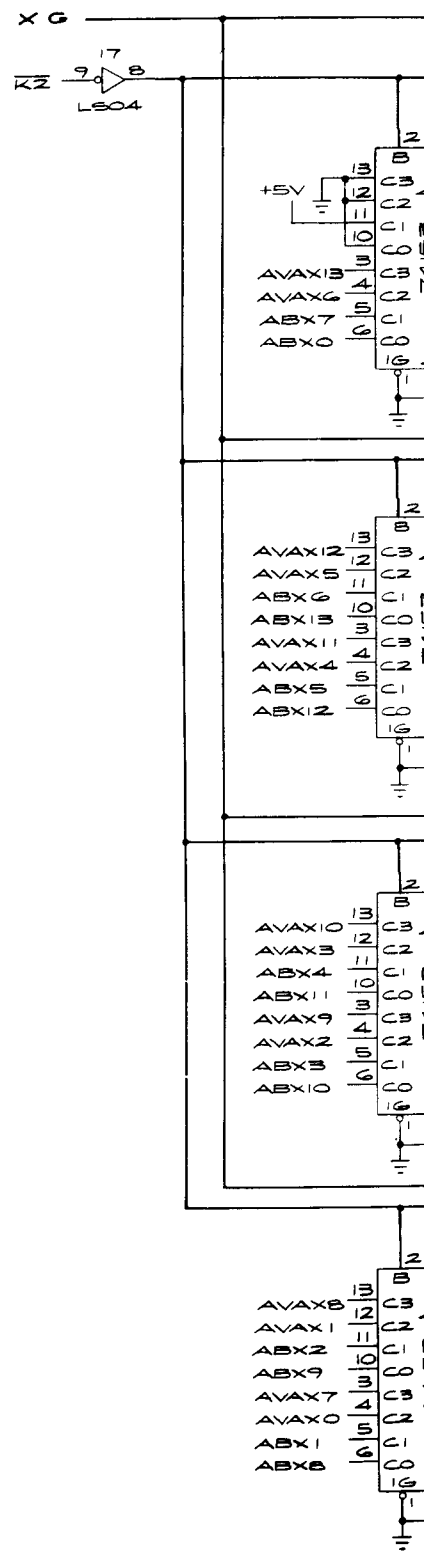
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# Dynamic RAM Data Selector

# Dynamic RAM

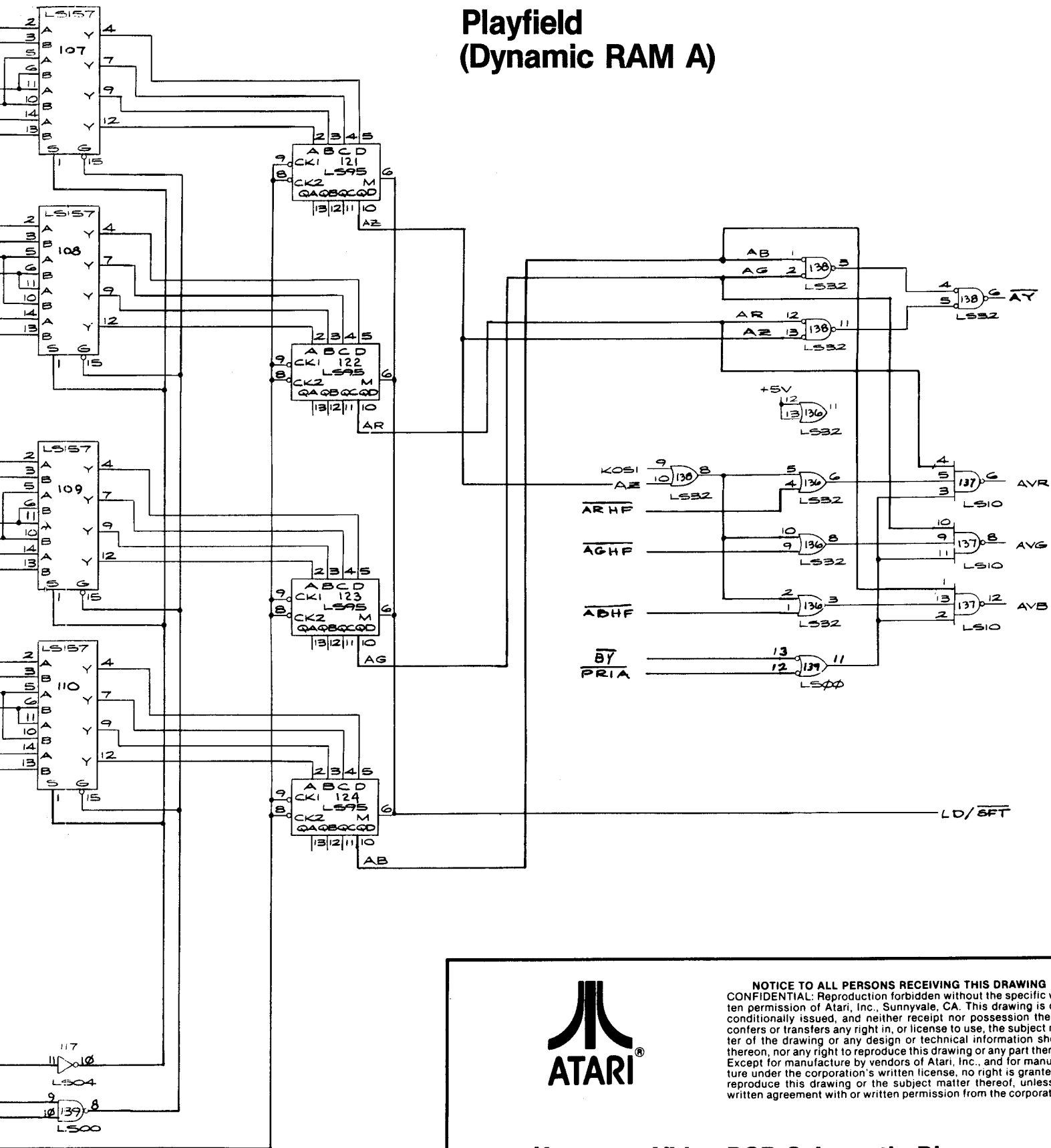


## Dynamic RAM Control Latches





# Playfield (Dynamic RAM A)



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## Kangaroo Video PCB Schematic Diagram

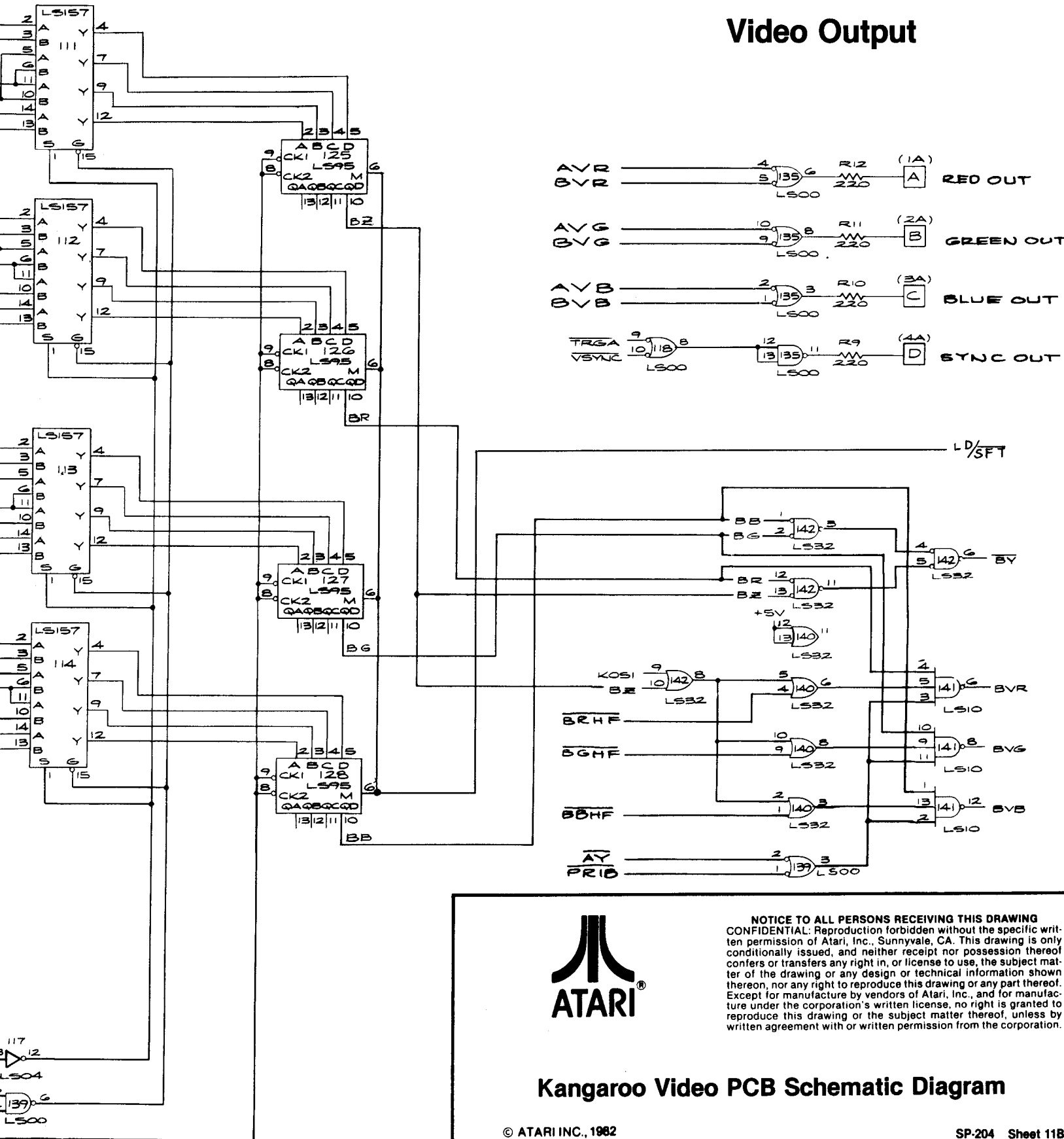
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# Video Output



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## Kangaroo Video PCB Schematic Diagram

# Motion Object (Dynamic RAM B)

