Regulator/Audio II PCB

The Regulator/Audio II PCB has the +5 VDC logic power to amplify the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage pass transistors Q3 and Q5's driver transistor that accurately regulates the logic power PCB by monitoring the voltage through the +5 VDC and ground inputs to the +5 VDC. Once adjusted, the voltage output remains constant at this voltage.

Regulator Adjustment

1. Connect the voltmeter between +5 VDC on the game PCB.
2. Adjust variable resistor R8 on the regulator PCB for a 5 VDC reading on the voltmeter.
3. If the voltage reading is incorrect, adjust the regulator by shifting the resistor to the appropriate harness on the game PCB.
4. Connect the voltmeter between +5 VDC and ground on the game PCB.

Audio Circuit

The audio circuit contains two amplifiers. Each amplifier consists of a 22-ohm resistor and an effective gain of 10.

Centipede Wiring Diagram (037432-01 C)
CAT Box Preliminary Set-up

1. Remove:
   - The electrical power from the game.
   - The wiring harness from the game PCB.
   - The game PCB from the cabinet.
   - The MPU chip G2 from the game PCB.

2. Connect:
   - The extender cables to the game PCB and the wiring harness.
   - The test points A0 and A2 on the game PCB.
   - The CAT Box flex cable to the game PCB test edge connector.

Diagnostic Tests

- **Instruction:**
  - Hold the main switch closed while setting the self-test switch to the on position.

- **Use of Test:**
  - The monitor displays the color hue adjustment pattern of 16 rectangles, as follows. Do not attempt any color hue or brightness adjustments unless you are a qualified color TV technician.
  - Pale Yellow/Green
  - Light Green
  - Dark Green
  - Deep Green
  - Black
  - Purple
  - Red
  - Royal Blue

- **Instruction:**
  - Activate any of the coin switches on the coin door.

- **Use of Test:**
  - A convergence pattern appears with a grid of white dots on a black screen. Do not attempt any convergence adjustments unless you are a qualified color TV technician.

- **Instruction:**
  - Set self-test switch to the off position.

- **Use of Test:**
  - Check output mode display and adjust brightness if necessary.

Power Input

Testing the RAM

1. Perform the CAT Box switch.
2. Set the CAT Box switch to:
   - Press TESTER RED
   - DBUS SOURCE T
   - BYTES TO 1024
   - W/ON
   - W/ON to WRITE
   - Key is 0000
   - Set W/ON MODE to 0
   - Set W/ON MODE to 0

3. If the CAT Box reads a **PARA ERROR LED** it shows the failing and the RAM switch is enabled.
4. If the **COMPARE ERROR LED** shows the failing and the RAM switch is enabled.

Sheet 1, Side B

Centipede™

Synchronizer
CAT Box Preliminary Set-Up
Power Input
Microprocessor
Address Decoder
RAM
ROM
Memory Map

Section of 037241-01

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TEST CONNECTOR-FOR ATARI CAT BOX

Microprocessor

Denotes a test point

RAM
Box preliminary set-up.
switches as follows:
1. RESET TO ADDR
2. (OFF)
3. To PULSE, then to OFF.
4. To PULSE, then to OFF.
Note an address that doesn’t compare, the COM-ED lights, the ADDRESS/SIGNATURE display address location, and the ERROR DATA Dis-
abled.
ERROR LED does not light, rekey 0000 and re-
the DBUS SOURCE switch set to A35D. This
data bits at address 0000 will go high. If the
RAM LED does not light after this step, the RAM

Memory Map

<table>
<thead>
<tr>
<th>Hex Address</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000-02FF</td>
<td>Payfield RAM</td>
</tr>
<tr>
<td>0300-07FF</td>
<td>Motion Object Picture</td>
</tr>
<tr>
<td>0700-07FF</td>
<td>Motion Object Vert.</td>
</tr>
<tr>
<td>0700-07FF</td>
<td>Motion Object Horiz.</td>
</tr>
<tr>
<td>0700-07FF</td>
<td>Motion Object Color</td>
</tr>
<tr>
<td>0800-0801</td>
<td>Option Switch 1 (0 = On)</td>
</tr>
<tr>
<td>0801-0801</td>
<td>Option Switch 2 (0 = On)</td>
</tr>
<tr>
<td>0C00-0C03</td>
<td>Vertical Mini-Trak Ball™ Inputs</td>
</tr>
<tr>
<td>0C04-0C07</td>
<td>Player 1 Joystick (PL, Down, Up)</td>
</tr>
<tr>
<td>0C08-0D0F</td>
<td>Custom Audio Chip</td>
</tr>
<tr>
<td>0D0F-0DFF</td>
<td>Payfield Color RAM</td>
</tr>
<tr>
<td>1000-10FF</td>
<td>Motion Object Color RAM</td>
</tr>
<tr>
<td>1400-14FF</td>
<td>Motion Object Control Latch</td>
</tr>
<tr>
<td>1600-16FF</td>
<td>EA ROM Address &amp; Data Latch</td>
</tr>
<tr>
<td>1700-17FF</td>
<td>EA ROM Read Data</td>
</tr>
<tr>
<td>1800-18FF</td>
<td>IRQ Acknowledge</td>
</tr>
<tr>
<td>1C00-1CFF</td>
<td>Left Coin Counter (1 = On)</td>
</tr>
<tr>
<td>1C00-1CFF</td>
<td>Right Coin Counter (1 = On)</td>
</tr>
<tr>
<td>1C00-1CFF</td>
<td>Player 1 Start LED (0 = On)</td>
</tr>
<tr>
<td>1C00-1CFF</td>
<td>Player 2 Start LED (0 = On)</td>
</tr>
<tr>
<td>1C00-1CFF</td>
<td>Task Ball™ Flip Control (0 = Player 1)</td>
</tr>
<tr>
<td>2000-2400</td>
<td>WATCHDOG</td>
</tr>
<tr>
<td>2000-2400</td>
<td>Clear Mini-Trak Ball™ Counters</td>
</tr>
<tr>
<td>2000-2FFF</td>
<td>Program ROM</td>
</tr>
</tbody>
</table>
Centipede Playfield RAM

Testing the Playfield RAM

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as follows:
   a. Press TESTER RESET
   b. DBUS SOURCE TO ADDR
   c. BITES to 224
   d. RW MODE to (OFF)
   e. RW to WRITE
   f. Key to 040
   g. Set RW MODE to PULSE, then to OFF.
   h. RW to READ
   i. Set RW MODE to PULSE, then to OFF.

3. If the CAT Box reads an address that doesn't compare, the COM- PARE ERROR LED lights, the ADDRESS/SIGNATURE display shows the falling address location, and the ERROR DATA DIS- PLAY switch is enabled.
4. If the COMPARER ERROR LED does not light, relay 0400 and repeat the test with the DBUS SOURCE switch set to ADDR. This ensures that the data bits at address 0400 will go high. If the COMPARER ERROR LED does not light after this step, the Play- field RAM is good.

Playfield Address Selector

The Playfield Address Selector controls the access to the playfield memory. It allows either the game MPU or the sync generator to scan the playfield memory. The Playfield Address Selector consists of multiplexers H5 and P7 and gate K4.

When BT pin 1 of P5 and P7 is low and pin 15 on P7 is low, the Playfield Address Selector receives BIT 15, 16, 32N, and 64H on P5 and 15, 16, 32N, 64N, and 128N on P7 from the sync generator. These signals enable the sync generator circuits to access the playfield memory.

When PRST goes high the game MPU addresses the playfield memory via A8B (A8B) for the positioning of the graphics. During horizontal blanking (pin 15 of P7 is high) the outputs of P7 (PRST4, PRST7) are held high enabling the motion object circuitry to access the playfield memory for the motion objects to be displayed.

Motion Object Circuitry (Vertical)

The Motion Object Circuitry (vertical) receives playfield data and vertical sync generator circuitry to generate the vertical component of the motion from the playfield memory and 1V-128V from the sync generator are connected. The output is gated by A7 when a motion object is on one of the sixteen latched positions of 16 to 18 and gate BT. A low on BT pin 6 indicates the presence of one of the vertical lines during non-active video time. This signal (MATCH) is sent to the motion object circuitry.

When 256H on pin 1 of D7 goes high, 14, 2V, 4V and PCD are selected in the latched output of ES is selected. The output of D7 is EXCLUSIVE OR gate E7 is PCD from the playfield code multiplex when high causes the output of E7 to be complemented. For example, if M PCD causes MSX2/MSX3 to go high. This causes the motion object video to bottom.

Sheet 2, Side A

Centipede™

Playfield Address Selector
Playfield Memory
Playfield Multiplexer
Picture Data ROM Circuitry
Motion Object Circuitry (Vertical)
Motion Object Circuitry (Horizontal)

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Testing the Option Switches
1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. RW to READ
   d. Key in address 0000 (H) or 0001 (H)
   e. RW MODE to STATIC
3. Activate the switch while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the switch is operating properly.

Coin Counter Output Circuit
This circuit consists of coin counter drivers Q6, Q7, and Q8 and data latch M10. The circuit is addressed by the MPU on A8-A0 and written by the MPU on data line D0. When the input to a driver is clocked high, its collector goes low grounding the return of the coin counter in the coin door.

Mini-Trak Ball™ Circuitry
Testing the Mini-Trak Ball™ Inputs
1. Perform the CAT Box Preliminary Set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. RW to READ
   d. Key in address 0000 (vertical) or 0001 (horizontal)
   e. RW MODE to PULSE
3. Spin the Mini-Trak Ball™ while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the Mini-Trak Ball input is operating properly.
Testing the Audio Outputs
1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. RW to READ
   d. Key in address 0100 (Hall-effect switch only) or 0001 (all others)
   e. RW MODE to DATATC
3. Activate the following player input switches one at a time, while monitoring the DATA DISPLAY:
   a. Coin Right
   b. Coin Left
   c. SLAM
   d. FIRE
   e. START 1
   f. START 2
4. The DATA DISPLAY will change if the switches are operating properly.

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
<th>RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>100F</td>
<td>00</td>
<td></td>
</tr>
<tr>
<td>100F</td>
<td>03</td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td>55</td>
<td></td>
</tr>
</tbody>
</table>
| 1001    | AP   | Pure tone is heard from channel 1 output.
| 1001    | 00   | Channel 1 output is turned off.
| 1002    | AP   | Pure tone is heard from channel 2 output.
| 1003    | 00   | Channel 2 output is turned off.
| 1004    | 55   |         |
| 1005    | AP   | Pure tone is heard from channel 3 output.
| 1006    | 55   | Channel 3 output is turned off.
| 1007    | AP   | Pure tone is heard from channel 4 output.
| 1007    | 00   | Channel 4 output is turned off. |

The video output circuit receives motion object, playfield, address and data inputs and produces a video output to be displayed on the game monitor. In order to read out of the color RAM, GR10Y and GR11Y from the motion object circuitry are multiplexed with AREA0 and AREA1 from the playfield circuit by E8. The output, selected by GR10Y or GR11Y is RAMA0-3 (RAM ADDRESS).

RAMA0-3 are applied to color RAM CB. The colors red, green, blue and an alternate color bit are outputs. The three color bits are latched by all as the game video in the three basic colors (or shades of gray in a black and white monitor). When the alternate color bit (CB pin 11) is active, an alternate shade of blue or green is available.

The following conditions, along with the various combinations of COLOR 1 (red), COLOR 2 (green), and COLOR 3 (blue), provide 6 extra colors for a total of 14.

1. If all pin 11 is low, transistor Q5 conducts and draws current from COLOR 1 and COLOR 2 are off.
2. If all pin 10 is low, transistor Q4 conducts and draws current from COLOR 1 and COLOR 3 are off.

High Score Memory Circuitry

The High Score Memory circuit stores the three best scores and other pertinent information. These scores are saved even if power is removed from the game. The High Score Memory circuit consists of an eraseable reprogrammable ROM E5, latches E4, E4, buffer H5 and timer A1.

A11 produces a 0.15V square wave at a 1V rate. This signal, when a 1V forward biased diode CR10 and allows capacitor CR9 to charge to ~15V. When the signal is 0V, CR10 is cut-off, and CR4 is forward-biased which causes CM to develop a charge. CR4 charges to approximately ~15V. This is the potential required for the ROM to operate.

The MPU addresses the EAROM (A00-AB0) when a low EA00/01 gates WRITE2 at gate A4. The trailing edge of the gated pulse latches the address information to the EAROM E5 via J4. Data is fetched by H4 at the same time. The EAROM mode (read, write or erase) is determined by decoding O92/093 at latch E4. A low EACON/ TD2R gates WRITE2 at gate A4. The trailing edge of this gated pulse latches the data into the EAROM E5 via latch H4.

Data read from the EAROM on pin 1 of buffer H4 goes low.