The UNDOSIC converts the analog values from the sensor to digital values that are sent to the microcomputer. The microcomputer then sends the data to the analog output matrix, which is controlled by the DAC. The DAC converts the digital values into analog values that are sent to the sensor.

The state machine can also instruct these counters to count up or down any specific number of counts. This will cause the beam to move a specific distance relative to where it was. During this movement, the beam is turned on or off, depending on the desired intensity. This is the procedure used to cause the beam to move to the left or right on the screen.

The vector to be drawn is specified by DX<10:10> from the memory device. Clock pulses will cause the counters to receive and whether the counters count up or down.

12-bit number (DVX0:11) is loaded into the counters from the vector position counters. Therefore, the position counters are two identical circuits. Therefore, the position counters contain rate multipliers (R0:10, 10:11) to latch down any specific number of counts. These will cause the beam to move a specific distance relative to where it was. During this movement, the beam is turned on or off, depending on the desired intensity. The vector to be drawn is specified by DX<10:10> from the memory device. Clock pulses will cause the counters to receive and whether the counters count up or down.

DVX0:11 memory data is loaded into rate multipliers R0:10, 10:11. The function that represents the horizontal location on the monitor screen and 10:11 being the far right side of the screen. The counter that is decreased is the left counter, respectively. The vector generated by DX<10:10> is to determine the screen position using the counter. The DX<10:10> determines whether the counters count up or down. The vector being drawn.

12-bit binary number that represents the horizontal location of the vector on the monitor screen and 10:11 being the far right side of the screen. The counter that is decreased is the left counter, respectively. The vector generated by DX<10:10> is to determine the screen position using the counter. The DX<10:10> determines whether the counters count up or down. The vector being drawn.
The purpose of the vector timer is to time out the length of time it takes to "draw" an actual vector on the monitor display. During the interval when the X- and Y-position counters are actually drawing the vector, STOP is high. This prevents the vector-generator state machine from advancing to its next state until the vector has been drawn, STOP goes low, allowing the state machine to advance to the next state in its intended sequence.

The vector timer consists of multiplexer F5, decoder E6, latch M6, adder M5, and counters B6, C6, and D6. M6 contains a scale factor which is added in M5 to the four timer signals. If TIMER0 thru TIMER3 inputs are any state but all high, decoder E6 directly decodes the sum and loads the decoder count into one of the loaded counters. When GO goes low, the counters count from the loaded count until the counters all reach their maximum count. At this time STOP goes low and clears the GO flip-flop of the state machine.

If the TIMER signals are all high, ALPHANUM goes low and data signals DVX1 and DVY1 are decoded by decoder E6. This is added to the scale factor and loaded into the counters.

The X- and Y-position counters down to counters (F10), and associated circuits, are a 12-bit binary counter with the decimal point of the binary number aligned on the left side of the display. The beam is turned on and off by the control circuitry in the state machine. The state machine is capable of using two different scanning cycles, one of which uses a "jump" feature for drawing "new" vectors. The beam is forced to the new position by using the "jump" feature, the beam position appearing on the last vector. The X and Y position counters are used as a 12-bit binary counter.
When the clock goes high, then the clock input to latch D goes high and stays high until the vector ROM or ROM matches (when WEN goes high), the vector ROM reads the microcomputer's address on the signal clocks. After this, the microcomputer's address is decoded by the microcomputer's address decoder, which is the same as the microcomputer's address decoder. The VCC input to the clock circuitry is a different 15 MHz clock.

When the vector ROM reads the microcomputer's address, the vector is decoded and the G0, G2, and G3 signals are output. When STOP is strobed through the G0, G2, and G3 signals, the STOP signal is decoded through the X position and Y position counters. When the STOP signal is decoded, the vector ROM is addressed. When a vector is selected, the VCC input to the clock circuitry is a different 15 MHz clock.

The state machine consists of input gates B8 and B9, ROM, and the microcomputer's address decoder. When the microcomputer's address is decoded, the signal D3 goes high, and clears the microcomputer's address decoder.

The state machine is the master controller of the vector generator, using the vector generator's ROM, to generate the vector's instructions. The vector generator's ROM is decoded by the vector generator's decoders, which are addressable by the vector generator's address decoder. The vector generator's address decoder is the same as the vector generator's address decoder. The state machine is the master controller of the vector generator.
Counters F4, H4 and J4 contain the address of the next data byte (instruction) to be fetched from the Vector Generator memory. Because these counters point to the next instruction in memory to be retrieved and performed, they are called the program counter. This program counter is incremented one count (to the next sequential address) each time the information at its current address is loaded into data latch 0 or data latch 2.

The program counter may also be preset to "return" to a previous address which it had stored in its "stack". The stack consists of register files F3, H3, & J3, and down/up counter K4. The stack is a 4-word 12-bit memory, used to save the contents of the program counter for future reference. It is loaded when DMAPUSH is low. Immediately after information is written into the stack, counter K4 increments one count. Immediately before loading the program counter from the stack, counter K5 decrements one count.

**STATE MACHINE**
The address selector consists of multiplexers F2, H2, J2 and K2. When \textit{VMEM} is low, the MPU of the microcomputer gains access to the address inputs of the vector generator memory. In this state, \textit{BUFFEN} is from \textit{\$2} and \textit{VW} (vector generator write) is low when \textit{\$2} and \textit{R/WB} are both low. When \textit{VMEM} is high, the address input to the vector generator memory is from the vector generator program counter and state machine. In this state, \textit{BUFFEN} and \textit{VW} are both held high by the pullup resistors connected to the 2B and 3B inputs of multiplexer K2.

Address decoder L2 decodes address bits A11 and A12, and selects the RAM or one of three ROMs of the vector-generator memory.

This address-selecting arrangement allows the game MPU to access the vector-generator memory, i.e., write data into the vector-generator RAM to instruct the vector generator what it should do next. The address selector can then allow the vector-generator program counter and state machine to access this same area of RAM also, and read what instructions were sent to it by the game MPU.
The data latches consist of latch 0 (H6), latch 1 (F6), latch 2 (J6), and latch 3 (K6). Inputs DDMA0 thru DDMA7 are the data outputs from the vector-generator memory.

Latches 0 thru 2 are directly clocked by the rising edge of the LATCH0, LATCH1, and LATCH2 outputs from the vector generator's state machine. Latch 3 is clocked by LATCH3 or by LATCH0, if ALPHANUM is low. Latch 0 is cleared when RESET, DMAGO, or ALPHANUM goes low. Latch 1 is cleared by ALPHANUM.