The High Score Memory circuit consists of an erasable reprogrammable ROM N9, latches L9, P9, N10 buffer M9, and timer N11.

N11 produces a 12KHz 0-15V squarewave. This signal when +15, forward biases diode CR4 and allows capacitor C50 to charge to -29V. When it's OV, CR4 is then cut-off and CR3 is forward biased which causes C49 to develop a charge. C49 charges to approximately -28V. This is the potential required for EAROM N9 to operate.

The MPU addresses the EAROM (AB0-AB5) via latch N10, when EAADDR goes high, and data is latched into the EAROM on DB0-DB7 through latch L9.

The function of the EAROM (read, write or erase) is determined by the MPU on data lines DB0-DB3. Latch D9 receives a high EACONTROL signal from the MPU address decoder and function data is passed to the EAROM.

Data in the EAROM is read by the MPU when the EARREAD is addressed by the MPU after a reset pulse or during self-test.
Program memory for the Asteroids Deluxe™ game is contained in three ROMs.

The RAM is the temporary storage area of the MPU and is enabled (Page enable) when low. When MPU is low, the RAM stores output (DB0 thru DB7) at the address defined by the MPU address bus (A8-A0). When R/WB is high, the MPU reads a byte at the addressed location.

The signal RAMSEL, will have the effect of swapping pages of the RAM. This allows greater flexibility.
POWER INPUT

This circuitry consists of the PCB inputs and outputs for the +5 VDC logic power and 25 VAC input to the onboard regulators. The +5 VDC inputs and outputs are discussed on Sheet 1, Side A of this schematic set.

The 25 VAC inputs are received by two full wave rectifiers. Diodes CR9 and CR8 rectify the negative cycle of the input and the 7915 regulates the voltage at -15 VDC. Diodes CR9 and CR10 rectify the positive pulse of the 25 VAC input and the 7815 regulates the voltage at +15 VDC. The 7812 regulates at +12 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR12 supplies the +8.2 VDC for the sample and hold circuit. The +22V (unregulated) is used to power operational amplifiers P11 and L8 in the audio output.
The address decoder performs the function of turning on or enabling the appropriate circuitry at the critical time, so that information can be transferred back and forth between the game circuitry and the MPU. The memory map below is for the Asteroids Deluxe™ game.

If you are going to use the Automatic RAM/ROM Tester, please remember to remove MPU C3 and ground the WDOG DISABLE test point.

### MEMORY MAP

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>R/W</th>
<th>DATA</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0</td>
<td>D7 D6 D5 D4 D3 D2 D1 D0</td>
<td>D7 D6 D5 D4 D3 D2 D1 D0</td>
<td></td>
</tr>
<tr>
<td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>R</td>
<td>Scratch RAM</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>Not used</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>3 KHz</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>VG halted</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>Shield switch</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>Fire switch</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>Siam switch</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>Left coin switch</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>Center coin switch</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>Right coin switch</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>1-player start switch</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>2-player start switch</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>Thrust switch</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>Rotate right switch</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>Option switch 8, 7 (at R5)</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>Option switch 6, 5</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>Option switch 4, 3</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>R</td>
<td>D</td>
<td>Option switch 2, 1</td>
</tr>
</tbody>
</table>

- POKEY
- EAROM read
- Start VG
- Latch EA address/data
- Watchdog reset
- Explosion pitch
- Explosion volume
- 3600 VG reset
- EA control latch
- 1-player start LED
- 2-player start LED
- Not used
- Ship thrust sound
- Bank select
- Left coin counter
- Center coin counter
- Right coin counter
- Noise generator reset
- Vector RAM
- Vector ROM
- Program ROM
- Program ROM
NOTE:
DO NOT USE split pads on PCB for troubleshooting purposes.

NOTE:
DO NOT USE split pads on PCB for troubleshooting purposes. If a 74LS244 is installed at location B1 and/or C1, the split pad for that location should be filled with solder. If a 74LS241 is used, the appropriate split pad should be open.
The circuitry of crystal Y1 and associated inverters provides the input to counters C3 and B3. Counters C3 and B3 count the frequencies necessary for the

**COUNTER**

A non-maskable interrupt counter causes an interrupt output of the MPU every 4 msec. The interrupt is derived from the 3KHz by a factor of 12 through counter C4. The interrupt occurs when pin 6 of inverter B4 goes low. During power-up, the interrupter is disabled by RESET. During Self-Test, the NMI

NOTE:
Either a 74LS245 or an AM8304B may be used at the +5V bus. Numbers not enclosed in parentheses.
CLOCK CIRCUIT

The clock circuit consists of inverters and counters C3 and B4. It reduces the crystal frequency down to the Asteroids Deluxe™ game.

NOTE:
The MPU in this game operates at a frequency of 1.5 MHz. Therefore the MPU chip must be the 6502A. The 6502's maximum frequency is 1 MHz and is not compatible with this game.

POWER RESET AND WATCHDOG COUNTER

During initial power-up, the delayed charging of capacitor C22 causes a preset of flip-flop D3 and a clear of counter D4. This results in holding RESET input to the MPU low. When the charge of C22 reaches about 1.5 VDC, preset and clear inputs are removed. Counter D4 counts to 128 at 3-KHz rate, and RESET is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

If the MPU program is operating properly, the MPU address decoding circuitry will output the WDCLR (Watchdog clear) signal at predetermined intervals. This serves to clear counter D4 before it counts up to the state that will create the RESET condition. If the MPU program strays from its intended sequence and does not output the WDCLR signal, counter D4 will count up to the RESET state and cause the MPU to return to its initialization routine.

NMI COUNTER

The NMI (non-maskable interrupt) input at the NMI input is used by the computer to disrupt occurs when the NMI counter is disabled by...