**Video Power Supply Wiring Diagram**

**Regulator/Audio PCB SCHEMATIC**

The Regulator/Audio PCB has the dual function of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

**Regulator Circuit**

The regulator consists of a voltage regulator Q1, a source power transistor Q3 and Q3's bias transistor regulator Q2. The Q2 has a biasing circuit which provides the necessary voltage for the regulator Q1 to regulate the game PCB by monitoring the voltage through feedback inputs to SENSE and SENSE'. The input voltage is directly from the +5 VDC and ground inputs to Q3. Q3 is the regulator. The regulator regulates the voltage of the game PCB. It eliminates a reduced voltage build-up on the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the voltage on the game PCB. Once adjusted, the voltage at the game PCB will remain constant at this voltage.

**Regulator Adjustment**

1. Connect a voltmeter between +5 V and GND test points of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio PCB for +5 V reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND test points of the Regulator/Audio PCB. Voltage reading shall be greater than +5.5 VDC. If greater, try cleaning connectors on both the game PCB and Regulator/Audio PCB.
4. If cleaning PCB edge connectors doesn't correct minus lead of voltage difference, contact minus lead of -5 VDC to GND test point of Regulator/Audio PCB and plus lead to GND test point of game PCB. Note the voltage and connect minus lead of voltmeter to +5 V REG test point on Regulator/Audio PCB and plus lead to +5 V test point on game PCB. From this you can see harness circuit is dropping the voltage. Troubleshoot harness wire or harness connector.

**Audio Circuit**

The audio circuit contains two independent amplifiers. Each amplifier consists of a TDA3110 amplifier with a gain of ten. In Asteroids, the DISABLE input to the PCB is permanently on. Therefore, this audio circuit is always on, even when the game is in the attract mode.

The audio circuit is repeated on Sheet 2, Side B, in more detail about its operation.

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**Drawing Package Supplement**

**Asteroids Operation, Maintenance, and Service Manual**

**Contents of this Drawing Package**

- Game Wiring Diagram, Coin Door and Power Supply: Sheet 1, Side A
- Microprocessor: Sheet 1, Side B
- Video Generator: Sheet 2, Side B
- Switch Inputs, Coin Counter, LED and Audio Outputs: Sheet 2, Side A

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CLOCK CIRCUIT

The clock circuit consists of crystal 11 and associated in-
verters and counters C1 and C2. Counters C4 and C5 count the
frequency down to the frequencies necessary for the
Asteroids game.

POWER RESET AND WATCHDOG COUNTER

During initial power-up, the delayed charging of capacitor C25
causes a preset of flipflop C4 and a clear of counter C5. This
results in holding RESET input to the MPU low. When the charge
of C25 reaches about 1.5 VDC, preset and clear inputs are remov-
ed. Counter C5 counts to 128 at 3 kHz rate and RESET is removed
from high from the input of the MPU. This allows the logic
power input to the PCB to stabilize before allowing the MPU to
begin its initialization routine.

If the MPU program is operating properly, the MPU address
decoding circuitry will output the WDDCL (Watchdog clear)
signal at predetermined intervals. This serves to clear counter C5
before it counts up to the state that will create the RESET condi-
tion. If the MPU program stays within its intended sequence and
does not output the WDDCLR signal, counter C5 will count up to
the RESET state and cause the MPU to return to its initialization
routine.

NMI COUNTER

The NMI (non-maskable interrupt) counter causes an interrupt
at the MPU input of the MPU every 4 microsec. The interrupt is
provided by dividing 3 kHz by a factor of 12 through counter C5. The
interrupt occurs when pin 9 of inverter 85 goes low. During power-up,
the counter is cleared by RESET. During self-test, the NMI is
disabled by TEST.

POWER INPUT

This circuitry consists of the PCB input and outputs for the 5 VDC
logic power and 36 VAC input to the on-board regulator. The 5 VDC in-
puts and outputs are discussed in Sheet 1, Side A of this schematic.

The 36 VAC inputs are received by two full wave rectifiers. Diodes CR9
and CR10 rectify the negative pulse of the input and the 7815 regulates
the voltage at -15 VDC. Diodes CR11 and CR12 rectify the positive
pulse of the 36 VAC input and the 7815 regulates the voltage at +15
VDC. The 7813 regulates at +12 VDC. The 7806 regulates an addi-
tional 5 VDC for the DACs. Zener diode CR14 supplies the +8.2 VDC
for the sample and hold circuit. The +24 V (unregulated) is used to
power operational amplifiers F11 and L10 in the audio output.

FROM SWITCH INPUTS SHEET 2, SIDE B

ROM/PROM CIRCUITRY

Program Memory for the Asteroids

DA10

F10

F11

PAUSE

F0

F1

PAUSE

F2

F3

SHEET 2, SIDE B

DP-143-02 3rd printing
Vector Generator Program Counter

State Machine

The state machine is the master controller of the vector generator system. It receives instructions from the game MPU via the vector generator RAM. It carries out these instructions by accessing the appropriate sections of the vector generator ROM memory, using the vector generator program counter to do so. The state machine reads the vector generator ROM data via Timer 0 and 2, and this data is decoded to determine how to proceed. Timer 0 is used to draw vectors, and Timer 2 is used to move the cursor to a new position. The vector generator has 32 memory addresses, and it is possible to access any of these addresses by selecting the appropriate position and counter. The vector generator has an 8-bit counter, which is incremented by the state machine. When the counter reaches a certain value, a new vector is drawn. The state machine has a 32-bit counter, which is used to keep track of the current position. The state machine has a clock signal that is used to synchronize the operations of the vector generator. The state machine has two output signals, one for the X axis and one for the Y axis. These signals are used to control the vector generator. The state machine has an input signal that is used to set the initial position of the vector generator. This signal is used to set the initial position of the vector generator. The state machine has a reset signal that is used to reset the vector generator. This signal is used to reset the vector generator. The state machine has a power signal that is used to power the vector generator. This signal is used to power the vector generator. The state machine has a reset signal that is used to reset the vector generator. This signal is used to reset the vector generator. The state machine has a clock signal that is used to synchronize the operations of the vector generator. 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no counters are two identical circuits. a description discusses only the X position counters contain rate multipliers (J and K), 49 and 89 multipliers (H, I, J, and K), and 13 and 14. The output of the downcounters is an x- y position counter. At the x-y position, the counters count down from the current position to the next position. The vector generator memory consists of 2K of ROM and 2K of RAM. It may be directly accessed by the MPU through the direct memory access (DMA) port. Data is written in from the MPU, and read out by the MPU when transferred to the MPU's DMA port. The 2K x 8 vector generator program memory chip resides in two 1K x 8 chips in locations D and E.

The X and Y position counters are activated when the screen is in the right position. At the current position, the counter counts down from the current position to the next position. The vector generator memory consists of 2K of ROM and 2K of RAM. It may be directly accessed by the MPU through the direct memory access (DMA) port. Data is written in from the MPU, and read out by the MPU when transferred to the MPU’s DMA port. The 2K x 8 vector generator program memory chip resides in two 1K x 8 chips in locations D and E. The data latches consist of latch 0 (L1), latch 1 (L2), latch 2 (L3), and latch 3 (L4). Latches 0 and 2 are directly linked to the right edge of the screen and the x-y position counters. Latches 1 and 3 are linked to the left edge of the screen. Latches 0 and 3 are linked to the top edge of the screen. Latches 1 and 2 are linked to the bottom edge of the screen. The latch 0 latches are selected by the counter and latch 2 latches are selected by the counter. Latch 0 is cleared when the screen is at 0. Latch 1 is cleared when the screen is at 1. Latch 2 is cleared when the screen is at 2. Latch 3 is cleared when the screen is at 3. The latch 0 latches are selected by the counter, latch 1 is selected by the counter, and latch 2 is selected by the counter. Latch 3 is selected by the counter.
INPUTS

PLAYER INPUT CIRCUITRY

DIAG STEP diagnostic steps. 3 KNI, SELF-TEST SLAM, HALT, FIRE and HYPER inputs are read by the MPU when SHRD switch input zero enables is low. Switches to be read are selected by AB3 thru AB2 from the MPU. All inputs are read on DB5. Switch inputs are active when pulled to ground. DIAG STEP, 3 KNI, and SELF-TEST signals are not read by the MPU to initiate and control the game's self-test procedure. SLAM is a signal read by the MPU to indicate the status of the associated switch mounted on the coin door. The MPU reads HALT to determine the state of the vertical generator.

The coin door and some control panel switches are read by the MPU when SHRP switch input one enables is low. Switches to be read are selected by AB3 thru AB2 from the MPU. All inputs are read on data line DB7. Switch inputs are "low" when pulled to ground.

OPTIONS INPUT CIRCUITRY

The game option switches are read by the MPU when OPTION switch enables is low. Switches to be read are selected by AB0 and AB1 from the MPU. Switch toggles 1, 3, 5, and 7 are read on DB2. Switch toggles 2, 4, 6, and 8 are read on DB1. Toggles inputs are "on" when pulled to ground.

VIDEO INVERTER

The video inverter circuitry is only used in a cocktail game. In an upright game, pin 19 is unconnected and therefore floats. When pin 19 floats, transistor Q16 is turned off and transistor Q17 is turned on. Therefore, INV is -9.2 VDC and NONINV is about 9.2 VDC. The result is a non-inverted X-axis and Y-axis output.

In a cocktail game, the wiring harness shorted connector J26's output pin 1 input pin 19. When the video for player 1 is being displayed, pins 7 and 19 are +5 VDC. This results in a non-inverted video output. When the video for player 2 is being displayed, pins 7 and 19 are grounded. This causes transistor Q16 to be turned on and Q17 to be turned off. Therefore, INV is 9.2 VDC and NONINV is -9.2 VDC. The result is an inverted X-axis and Y-axis output, causing the monitor's display to be upside down.

OUTPUTS

M10 latches control signals to enable different sounds.

The THUMP sound is heard throughout play. The 556 is connected as an oscillator, enabled by NF pin 2. The frequency is determined by the current coming out of Q2. This depends on its base voltage, which is derived from the four-bit code in NF.

The SAUCER sound is heard when an enemy saucer appears. The 556 is a voltage-controlled oscillator. Its modulating voltage is derived from the 556. The 556 is a low-frequency oscillator. The effect is a warbling sound. SAUCERX changes some component values, in order to provide for 2 different saucer sounds.

The FIRE sounds for the Saucer and the Space Ships are generated by two identical circuits. Each contains a 555 operating as a voltage-controlled oscillator. The saucer Fire sound is initiated by SAUCERFIRE, and the Space Ship Fire sound is initiated by SPACEFIRE. Each of the 555s is configured in such a way that when they are enabled, they output a signal of a specific frequency and amplitude. This signal begins to decay immediately, both in frequency and amplitude, due to the discharge of the control capacitors (C35 & C36). The 555s are placed in series to obtain the desired 12 kHz frequency.

The EXPLODE sound is heard when any objects, on impact, are sampled at a frequency by P1 and control switches. The frequency changes in conjunction with the sound's level and rate, as defined by the game's programming. The NF is modulated in 13 kHz.

R9 and P9 generate random noise. This noise is filtered by R11 and produces the rumble sound heard when the ship is thrusting.