Drawing Package Supplement
to
ASTEROIDS DELUXE™
CABARET
Operation, Maintenance and Service Manual

Contents of this Drawing Package

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NOTICE TO ALL PERSONS READING THIS DRAWING

This drawing is the property of Atari, Inc. and is intended for use as a pattern for wiring, construction and assembly only. This drawing may not be duplicated, copied, reproduced, or used in whole or in part for any purpose other than manufacture of the equipment shown on this drawing without written permission from Atari.
REGULATOR/AUDIO I PCB SCHEMATIC (034485-03 A)

Regulator/Audio I PCB

The Regulator/Audio I PCB has the dual functions of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage regulator Q1, current source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through high-impedance inputs SENSE and —SENSE. The inputs are directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage on the game PCB. This eliminates a reduced voltage due to IR drop in the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the +5 VDC on the game PCB. Once adjusted, the voltage at the input of the game PCB will remain constant at this voltage.

Regulator Adjustment

1. Connect a voltmeter between +5 V and GND test points of the game PCB.
2. Adjust variable capacitor R8 on the Regulator/Audio I PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND on the Regulator/Audio I PCB. Voltage reading must not be greater than +5.5 VDC. If greater, try cleaning edge connectors on both the game PCB and the Regulator/Audio I PCB.
4. If cleaning PCB edge connectors doesn't decrease voltage difference, connect minus lead of voltmeter to GND test point of Regulator/Audio I PCB and plus lead to +5 V REG test point on Regulator/Audio I PCB. Now connect minus lead of voltmeter to —5 V REG test point on game PCB. From this you can see which harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

Audio Circuit

The audio circuit contains two independent audio amplifiers. Each amplifier consists of a TDA2002AV amplifier with a gain of ten.

DIAGRAM (036352-01 A)

Denotes a test point

AMERICAN-MADE COIN DOOR SCHEMATIC (034988-01 A)

BRITISH-MADE COIN DOOR SCHEMATIC (037050-01 A)
CLOCK CIRCUIT

The clock circuit consists of crystal V1 and associated inverters and counters C3 and C4. Counters C3 and C4 count the crystal frequency down to the frequencies necessary for the Asteroids Deluxe™ game.

NOTE:
The MPU in this game operates at a frequency of 1.1 MHz. Therefore the MPU chip must be the 6502A. The 6502's maximum frequency is 1 MHz and it is not compatible with this game.

POWER RESET AND WATCHDOG COUNTER

During initial power-up, the delayed charging of capacitor C22 causes a preset of flip-flop C3 and a clear of counter D4. This results in holding RESET input to the MPU low. When the charge of C22 reaches about 1.5 VDC, preset and clear inputs are removed. Counter D4 counts to 128 at 3 kHz rate, and RESET is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

If the MPU program is operating properly, the MPU address decoding circuitry will output the WOOLER (watchdog clear) signal at predetermined intervals. This serves to clear counter D4 before it counts up to the state that will cause the RESET condition. If the MPU program strays from its intended sequence and does not output the WOOLER signal, counter D4 will count up to the RESET state and cause the MPU to return to its initialization routine.

NMI COUNTER

The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 usec. The interrupt is derived by dividing 3 kHz by a factor of 12 through counter D4. The interrupt occurs when pin 6 of inverter B4 goes low. During power-up, the NMI counter is disabled by RESET. During self-test, the NMI is disabled by TEST.

POWER INPUT

This circuitry consists of the PCB inputs and outputs for the +5 VDC logic power and 25 VAC input to the on board regulators. The +5 VDC inputs and outputs are discussed in Sheet 1, Side A of this schematic set.

The 25-VAC inputs are received by two full wave rectifiers. Diodes CR1 and CR2 rectify the negative cycle of the input and the 7905 regulates the voltage at +5 VDC. Diodes CR3 and CR4 rectify the positive pulse of the 25 VAC input and the 7905 regulates the voltage at +15 VDC. The 7809 regulates at +12 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR5 supplies the +3.3 VDC for the sample and hold circuit. The +22 VDC (regulated) is used to power operational amplifiers P1 and L8 in the audio output.

ROM/PROM CIRCUITRY

Program memory for the Asteroids Deluxe™ game is contained in three ROMs.

RAM CIRCUITRY

The RAM is the temporary MPU and is enabled when Page enabled is low. When MPU is low, the RAM strobe (D0 thru D7) at the byte by the MPU address bus at the R/WB high, the MPU reads byte at the addressed location.

The signal RAMSEL reflects the fact of swapping page RAM, this allows greater flexibility.
Counters F4, H4 and J4 contain the address of the next data byte (instruction) to be fetched from the Vector Generator memory. The next instruction in memory to be retrieved and performed, they are called the program counter. This program counter is incremented one count to the next sequential address each time the information at its current address is loaded into data latch 0 or data latch 2.

The program counter may also be preset to “jump” to a new address. This new address can be loaded into the program counter from the vector generator memory via data latches F6 and H6 and buffers H5 and J5.

The program counter may also be preset to “return” to the previous address which it had stored in its “stack.” The stack consists of register files F3, H3, F4, H4, and J3, and J4, and J5, and J6, of the CPU. The stack is a 4 word 12-bit memory, used to save the contents of the program counter for future reference. It is loaded when the program counter is free. Whenever the stack counter K4 increments one count, it immediately transfers the contents of the stack to the program counter.

The program counter may then also transfer the contents of the “jump” to a new address. This new address can be loaded into the program counter from the vector generator memory via data latches F6 and H6 and buffers H5 and J5.

The state machine is the “master controller” of the vector generator circuitry. It receives instructions from the game MPU, via the game vector generator RAM. It carries out these instructions by accessing the appropriate sections of the vector generator ROM memory, using the vector generator program counter to do so. The state machine reads the vector generator ROM data (via ISA bus) and decodes this information to determine how it should use this data. 1) to draw a vector, 2) to move the monitor beam to a new position on the monitor display, 3) to “jump” to a new vector memory address, 4) to return to a previous vector memory address, 5) to tell the game MPU that it has completed its current instructions, and is waiting for its next command.

The state machine consists of input gates B8 and E5, ROM C8, latch D6, clock circuitry A6, and decoder E2. Four-bit input TIMERS thru TIMERS is the operation code input to the state machine. The A4 thru A6 address input to ROM C8 tells the ROM which instructions to perform. Address inputs A6 thru A3 from latch D8 tells the ROM which state was last performed. The address A7 input to D6 tells the ROM that the position counters are presently drawing a vector. The HALT input to A7 tells the ROM that the vector generator has completed its operations.

During initial power-up of the game, the HALT signal is present low. The microcomputer reads the high HALT signal through its switch input port (maximally 1.0s) on data line DB7. This tells the microcomputer that the vector generator is halted and waiting for an instruction. To ensure that the beam is off when the state machine is halted, the high HALT clocked through latch D8, results in a low BLANK to the Z-axis output.

The microcomputer outputs an address that results in a DMAO signal that causes RACT to go high, and clears the vector generator data latches. This makes TIMERS thru TIMERS signals all low. The state machine now begins executing instructions, starting at vector memory location 0.

When the state machine receives the operation code for a RACT instruction, it outputs a low RACTH signal, setting the HALT flip-flop A6 and suspending state machine operation.

The GO signals load and enable the vector timer and the X and Y position counters and tell the ROM that the vector generator is now actively drawing a vector. The HALT input to the GO flip-flop A6 sets the outputs to ensure that the vector timer and position counters are not active. When the state machine is halted, when a low COSTROBE is clocked through A6, the vector timer and X and Y position counters begin to operate from the GO, SD and OD signals. When STOP is clocked through A6, the vector timer has its maximum count, and GO goes high. This means the vector has been drawn.

The VGOK input to the clock circuitry is a buffered 1.5MHZ clock signal from the microcomputer. This is the same frequency used to clock the MPU of the microcomputer. The signal clocks latch D8 unless the microcomputer is addressing the vector RAM or ROM memories (when VMEM goes low). Then the clock input to latch D8 goes high and stays high until VMEM goes high.

The purpose of the vector timer is to time out the maximum length of time it takes to “draw” an actual vector on the monitor display. During the interval when the X- and Y-position counters are actually drawing the vector, STOP is high. This prevents the vector generator state machine from advancing to its next state until the vector currently being drawn is completed. As soon as the vector has been drawn, STOP goes low, allowing the state machine to advance to the next state in its intended sequence.

The vector timer consists of multiplexer F5, decoder E6, latch M6, adder M5, and counters E6, C6, and D6. M5 contains a scale factor which is added to M5 in the four timer signals. If TIMERS thru TIMERS inputs are any state but all high, decoder E6 directly decodes the sum and loads the decoded low into one of the counters. When GO goes low, the counters count from the loaded count until the counters all reach their maximum count. This count is a maximum length of 1024. At this time STOP goes low and clear the GO flip-flop of the state machine.

The output signals are all high, A1PNUMER goes low and data signals E1X1 and E1Y1 are decoded by decoder E6. This is added to the scale factor and loaded into the counters.

The X- and Y- position counters are A- and B-type counters. The A-type counter is made up of four two-state flip-flops, one for each position. The B-type counter is made up of four two-state flip-flops, one for each position. The B-type counter is used to ensure that the position signal remains valid, even if the vector generator state machine advances to a new state.
X- AND Y-POSITION COUNTERS

- X and Y position counters are two identical circuits. Therefore, the description describes only the X-position counters.
- X-position counters contain rate multipliers (M, M and MB), multipliers (M, M, and MB), which are associated with six (8 and 16). The output of the downstage is a 12-bit number that represents the horizontal line of the screen. The horizontal line number is the right side of the screen. If the number is 1023, the output will count the next position to the right or left of the screen.
- The vector generator circuit includes instructions from its memory and then it's using that data to alter the binary count of these counters in eXe.

The X and Y position counters are updated continuously, i.e., the vector from a different starting position when the vector is updated. When the beam is "jumping," the beam itself is turned off to prevent unwanted lines from appearing on the screen. To prevent this new position from being drawn, a generator causes the beam to go to low. At this time, a new 12-bit number (DVX-Y) is loaded into the counters from the vector generator memory data latches.

The state machine can also instruct these counters to count up or down any specific number of counts. This will cause the beam to move to the left or to the right a specific number of counts. During this movement, the timer is locked on with the desired position, and then it's using that data to alter the binary count of these counters in eXe.

The state machine can set these counters to an entirely different position from their previous contents. This will cause the beam to be placed at a new location on the monitor screen. After this, the beam position is updated and then it's using that data to alter the binary count of the counters in eXe.

The A for the X and Y position counters is the signal to A for the vector generator memory. The B for the X and Y position counters is the signal to B for the vector generator memory.

The D for the X and Y position counters is the signal to D for the vector generator memory.

The E and X and Y position counters are updated continuously, i.e., the vector from a different starting position when the vector is updated. When the beam is "jumping," the beam itself is turned off to prevent unwanted lines from appearing on the screen. To prevent this new position from being drawn, a generator causes the beam to go to low. At this time, a new 12-bit number (DVX-Y) is loaded into the counters from the vector generator memory data latches.

The state machine can also instruct these counters to count up or down any specific number of counts. This will cause the beam to move to the left or to the right a specific number of counts. During this movement, the timer is locked on with the desired position, and then it's using that data to alter the binary count of these counters in eXe.

The state machine can set these counters to an entirely different position from their previous contents. This will cause the beam to be placed at a new location on the monitor screen. After this, the beam position is updated and then it's using that data to alter the binary count of the counters in eXe.

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The D for the X and Y position counters is the signal to D for the vector generator memory.

The E and X and Y position counters are updated continuously, i.e., the vector from a different starting position when the vector is updated. When the beam is "jumping," the beam itself is turned off to prevent unwanted lines from appearing on the screen. To prevent this new position from being drawn, a generator causes the beam to go to low. At this time, a new 12-bit number (DVX-Y) is loaded into the counters from the vector generator memory data latches.

The state machine can also instruct these counters to count up or down any specific number of counts. This will cause the beam to move to the left or to the right a specific number of counts. During this movement, the timer is locked on with the desired position, and then it's using that data to alter the binary count of these counters in eXe.

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The state machine can also instruct these counters to count up or down any specific number of counts. This will cause the beam to move to the left or to the right a specific number of counts. During this movement, the timer is locked on with the desired position, and then it's using that data to alter the binary count of these counters in eXe.
**INPUTS**

**PLAYER INPUT CIRCUITRY**

DIAG STEP (diagnostic step), 3 KV, SELF-TEST SLAM, HALT, FIRE, and SHIELDSD switches are read by the MPU when SIMP switch is pressed. Swiches to be read are selected by A0 and A0 from the MPU. All inputs are read on DB7. Switch inputs are active when pulled to ground. DIAG STEP, 3 KV, and SELF-TEST are signals read by the MPU to initiate and control the game's self-test procedure. SLAM is a signal read by the MPU to indicate the status of the anti-stain switch mounted on the coin door. The MPU reads HALT, to determine the state of the vector generator.

The coin door and some control panel switches are read by the MPU when SIMP switch is pressed. Switches to be read are selected by A0 and A0 from the MPU. All inputs are read on data line DB7. Switch inputs are "on" when pulled to ground.

**OPTIONS INPUT CIRCUITRY**

The game option switches are read by the MPU when SIMP switch is pressed. Switches to be read are selected by A0 and A0 from the MPU. Switches toggle 1, 3, 5, and 7 are read on data line DB6 and toggles 2, 4, 6, and 8 are read on DB1. Toggles input are "on" when pulled to ground.

**VIDEO INVERTER**

The x- and y-video inverter circuits are identical; therefore, only the x-video inverter circuit is explained. For inverted video output, pin 19 is grounded which turns on transistor Q13 and turns off transistor Q12. In this state INV is +0.2 VDC and NONINV is -0.2 VDC.

For a noninverted video output, pin 19 is unconnected and floats. In cocktail games, pins 19 and 7 are shorted and have a potential of +5 VDC. This causes transistor Q13 to be cut off and transistor Q12 to be turned on. INV is then -0.2 VDC and NONINV is approximately +0.2 VDC.

In upright games, only the x-video inverter is used. In cocktail games both x- and y-video inverters are used, and in cocktail games video inversion is not necessary, so neither is used.

**OUTPUTS**

**The Custom Audio Chip M78**

The Custom Audio chip M78 generates most of the sounds for Asteroids Deluxe®.

R/W determines the direction of data flow (DB0-DB7) as addressed by A0-A0. When R/W is high, the MPU reads the input data from DIP switch LS. When R/W is low, the MPU writes the audio I/O instruction for an output.

The 42 input from the MPU is the operating frequency for the audio I/O chip and sets the timing for data bus lines DB0-DB7.

When P1=0, A16, and A17 are high, the audio chip select pulse is gated to the audio I/O chip. This pulse prepares the audio I/O for operation.

**EXPLODE**

The EXPLODE sound is heard when any object explodes. Noise is sampled at a frequency determined by P7, and control bits EXPITCH and EXPITCH. Changing the sampling rate changes the pitch of the explosion. The noise is amplified and modulated in R6 by EXPAUD and EXPAUD.

R6 and R6 generate random noise. This noise is filtered by P13 and produces the rumble sound heard when the ship is throttling.
LAMP, LED, AND COIN COUNTER OUTPUT

This circuit consists of coin counter drivers Q8, Q9, Q10, and data latch M10, controlled by the microcomputer's address decoder. When the input to a driver is clocked high, its collector goes low, grounding the return of the coin counter in the coin door.

When START1 or START2 is clocked low, it grounds the START LEDs in the control panel.

VIDEO OUTPUTS

The video-output circuit consists of three individual circuits: X-axis, Y-axis, and Z-axis. The X-axis and Y-axis video-output circuits each consist of a digital-to-analog converter (DAC), current-to-voltage converter, two sample and holds, and an amplifier. The Z-axis video-output circuit consists of a shift register and a summer.

X and Y Outputs

The DACs (D11 and D12) each receive binary numbers from the vector generator's position counter outputs. These numbers represent the location of the beam on the monitor. For the non-inverted X axis, the numbers range from 0 to 1023, where 1023 is at the right edge of the monitor screen, 512 is at the center, and 0 is at the far left. For the non-inverted Y axis, the numbers range from 128 to 996, where 996 is at the bottom of the monitor screen, 512 is at the center, and 128 is at the top. When the X and Y axes are inverted, the monitor picture is turned upside down. This is used for a two-player cocktail game.

The DACs convert these binary numbers to current outputs. The DAC's current outputs are applied to the pin6 inputs of current-to-voltage converters C12 and C13.

The current-to-voltage converters, the signal is fed to two sample-and-hold circuits. One is non-inverted and the other is inverted. The non-inverted sample and hold consists of one stage of analog switch D12 and capacitor C69 for the X axis, and B12 and C69 for the Y axis. The inverted sample and hold consists of inverter E12, one stage of analog switch D12, and capacitor C68 for the X axis and B12, B12 and C10 for the Y axis.

The sample-and-hold circuits are controlled by SHCON (sample and hold control). SHCON is derived by gating 3 MHz from the microcomputer's clock circuitry and VCC' from the vector generator's state generator. The result of these inputs is that the non-inverted and inverted analog signals applied to the analog switches have sufficiently stabilized before being applied to the sample-and-hold capacitors.

The output swing of SHCON is +8 to +8 VDC. When SHCON is high, the voltage charges or discharges the sample-and-hold capacitors to X and Y analog voltage value. The voltages are then applied to the inputs of the second analog switch. These switches select either the non-inverted or inverted X-axis and Y-axis outputs. The outputs are then amplified by the second stages of C12 and C13 for an input-matched output to the X and Y inputs to the monitor. Since the monitor doesn't have fixed adjustable X and Y gains, the gains are adjustable by variable resistors R102 and R126.

Z Output

The Z-axis video output receives six inputs: BVLDR (beam valid), from the output of the vector generator's position counters, tells the Z-axis to draw the line, B11 (vector line valid), from the vector generator's state machine, tells the Z-axis to stop drawing a line. SCAL (scaled) and SCAL (scaled) (one of the outputs of the vector generator's scaling logic), tell the Z-axis to scale the BVLDR signal by a factor of 2 or 4. The BIVLDR and B11 signals are applied to the inputs of the analog switch. The output of the analog switch is then applied to the Z-axis output, which is then amplified and applied to the Z input of the monitor. Since the monitor doesn't have fixed adjustable X and Y gains, the gains are adjustable by variable resistors R102 and R126.

Noise is introduced at the start-up of transistor Q3. This allows the scale inputs to be passed through transistor Q2. When B11 is low and B11 is high, the output of transistor Q3 turns on, and the signal is grounded at the base of transistor Q2.

The scale inputs at the base of transistor Q1 determine Q1's emitter voltage, during the line-draw period. The R109 thru R104 resistors R109 thru R104, resistor R102, and resistor R100 result in a range of about +1.0VDC when the line is complete and about +0.0VDC when the line is incomplete. The emitter of transistor Q1 follows at about +1.0 VDC, while the emitter of transistor Q2 follows at about +0.0 VDC. This input is applied to the Z input of the monitor. Since there are brightness and contrast controls in the monitor, there are no adjustments in this circuit.