ELECTRONIC IN-CIRCUIT PCB TESTERS
&
IDENTIFIER PCB TESTER

by

W.P.Kotze

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SUMMARY

Various types of electronic card test equipment are freely available today for different types of electronic printed circuit boards. A company certainly wants to pick the most suitable tester to suit their needs, and more importantly a tester that will fit into their budget. Today a company can easily import in-circuit testers that will cost well in the region of six figures. The cheaper the equipment go, the less features one can expect from the equipment. Like all other big decisions in life, this might also be a tough one for a company.

Part one of this thesis will consider most of these questions, and will also give more insight on what type of specifications to look for. This section will also explain the different types of faults that occur, the repair costs involved, different types of card testers available and some of their features. Advanced in-circuit testing techniques will also be explained.

Part two of this thesis describes the design and development of the Identifier Card Tester. The "Program Control and Impulse Sender Card", (referred to as "Identifier Card") is one of the cards used in a system called "Electronic Identifier".

The electronic identifier was developed to enable a subscriber directory number, a line or equipment numbers, or in general, the origin of information and classes-of-service to be determined by way of an existing connection within a telephone exchange. The system was designed for the purpose of incorporating it into the existing public exchanges where no identifier wires are available. It operates on the principle of a switching circuit (line) tester. The identification pulses are evaluated with the aid of 6 mm bistable magnetic ring cores according to the current steering principle. The program control and the output circuit uses a transistor, a magnetic core/transistor or a magnetic core/thyristor circuit.

The electronic identifier is mostly used with "Routiners" in Electro-mechanical exchanges. The biggest percentage of failures on these systems are caused by the Identifier Card and hence the request for the development of a "Identifier Card Tester".

SCOPE

PART 1:
To investigate the techniques and features of the differen types of Card Testers available.

PART 2:
To describe the design and development of the "Identifie Card Tester".

CONTENTS

PART 1: LIST OF FIGURES :

PART 2: LIST OF FIGURES :

1.0 INTRODUCTION

There are two types of repairs or testing:
The first type will be just after assembly, (a new factory card) and the other type will be a card already in use. The two types of repairs will not have the same major fault categories, and therefore the two repair or testing lines will be different.

1.1 TYPES OF PC FAULTS AFTER ASSEMBLY:

It appears that two major fault categories may be found after assembly, namely Catastrophic faults and Dynamic faults.

1.1.1 CATASTROPHIC FAULTS:

FAULTS	SYMPTOMS	MOST COMMON CAUSES	OCCURRENCE
Shorts	* Electrical conduction in the wrong place.	* Solder process. * Mechanical defect.	25% - 75%
Dry-joints	* No electrical conduction where there should be.	* Over etched tracks. * Mechanical defects. * Solder process. * Repair process.	5% - 25%
Wrong component	* Component installed in the wrong place.	* Possible human error.	10% - 25%
Backward component	* Improperly mounted component.	* Possible human error.	5% -20%
Out of tolerance	* Value of part does not meet specification.	* No incoming inspection.	20% - 40%
Missing Component	* Component not installed.	* Possible human error.	10% - 20%
Dead or partially dead device	* Defective component	* No incoming inspection. * Exposure to heat during solder or repair process. * Infant mortality.	10% - 40%

1.1.2 DYNAMIC FAULTS:

FAULTS	SYMPTOMS	MOST COMMON CAUSES	OCCURRENCE
Dynamic on the component level.	* Too slow device * Set up and hold problem. * Cycle time problem.	* No incoming inspection. * Change in vendors.	1% - 10%
Dynamic on the board level.	* Interactive/ functional problems involving the communication between two or more devices.	* Usually some tweaking of a design which is pushed to its limits and/or the combined results of component level dynamic problems.	1% - 10%

1.2 TYPES OF FAULTS DURING FIELD-SERVICE:

Also two types of fault categories:

1.2.1 Catastrophic faults:

FAULTS	SYMPTOMS	MOST COMMON CAUSE	OCCURRENCE
Shorts.	*Electrical conduction in the wrong place.	* Component failure. * Dust & moisture.	1% - 10%
Dry-joints.	*No electrical connection where there should be.	* Bad solder. * Lightning. * Corrosion. * Component failure.	1% - 10%
Wrong component.	*Component installed wrong place or wrong component installed.	* Possible human error.	less than 1%
Out of Tolerance.	*Value of part does not meet the specification any more.	* Age of device.	1% - 10%
Dead or partially dead.	*Defective component.	* Age of device.	20% - 40%

1.2.2 Dynamic faults:

FAULTS	SYMPTOMS	MOST COMMON CAUSE	OCCURRENCE
Dynamic on the component level.	* Too slow device. * Not enough drive power from device.	* Breakdown of device.	1% - 5%
Dynamic on the board level.	* Interactive/ functional problems involving the communication between two or more devices.	* Combined result of components. * Age of device.	less than 1%

1.3 REPAIR COST:

The repair cost of PC faults will follow a theory known as the base ten logarithmic rule. This means the cost to test and repair PC faults in the industry increases by one order of magnitude when moving through each successive level of testing or repairing.
Example:

Assume that the cost to test for and repair a PC fault at the incoming inspection level is five cents.

Level of test or creation	Cost of test and repair
During incoming inspection.	R 0.05
At the in-circuit tester.	R 0.50
At the next level of board test.	R 5.00
At system level.	R 50.00
In the field.	R500.00

This example points out the importance of locating PC faults at the earliest possible stage of test or creation, and therefore the user must select the most cost effective and efficient automatic test equipment (ATE) for his specific needs.

A conventional in circuit tester (FACTRON 333E) can cover all the "catastrophic" problems. But if 50 percent of the "catastrophic" problems are shorts, then it becomes cost effective to pre test the PC boards on a shorts tester (FACTRON 4400) before testing on the in circuit tester. The shorts tester is much less expensive than the in circuit tester.

A functional tester (FACTRON 720) can cover all board problems, but it's being designed to cover dynamic performance and dynamic timing problems. A high performance in circuit tester (FACTRON 730) is designed to effectively cover all catastrophic problems and more! It also covers a category of component dynamic problems previously only addressed by the functional level of test. Off loading faults from any higher level of test is always advantageous. Therefore a high performance in circuit tester in front of a functional tester can provide a very cost effective test technique.

Conventional in circuit testers are positioned to capture catastrophic problems relating to connections and components where high performance in circuit testers are positioned to not only capture both catastrophic problems involving connections components, but also extend their fault coverage to include those component faults which are dynamic in nature.

2.0 DIGITAL TEST EQUIPMENT

2.1 SIXTEEN-PIN LOGIC MONITOR:

It's a efficient approach to check the operation of digital ICs. The bottom of this device clips over a 14- or 16-pin IC and the top contains a number of LEDs, corresponding to the number of IC pins. Each pin goes to a high impedance, 100 KΩ go/no-go detector. A 2-volt threshold causes the LED to be turned on. This logic monitor works with any kind of DTL, TTL, HTL, or CMOS logic. A power-seeking gate network automatically finds the power supply leads and feeds Vcc to the internal circuits of the logic monitor itself.

The entire unit is 100mm long. Each of the LEDs is labelled with the corresponding pin number, so that the user can use the logic diagram of the particular IC to determine whether he is looking at a logic input, output, a NOR or NAND gate, or at the input or output circuit of a flip-flop. This device is a relatively inexpensive means of rapidly checking the static logic operation as well as those occurring under low-speed toggling conditions. At a glance a test engineer can see what the IC does, pin by pin on the logic monitor.

Advantages:

* Requires no battery.
* Handy for a lot of IC troubleshooting.
* It's relatively cheap. (± R200)

Disadvantages:

* The input impedance will be too low for some types of logic ICs and might load the circuit, causing unwanted operation (etc. if the IC drive its maximum input loads (fan-out).
* Only suitable for low speed operation.

2.2 TRENDAR-FAULTRACK 200:

The basic feature that makes the Trendar-Faultrack 200 different is that it compares two identical ICs, pin by pin, in the same circuit. Like the logic monitor, this device is hand held and clips over any 16-pin DIP IC. On the tester there is room for a separate IC identical to the one being tested to be plugged in. In typical operation, both ICs, the one under test and the one plugged in as the reference, are stimulated by the same inputs. Their outputs are compared in real time by built-in comparator circuits.

When the logic levels at any two pins do not correspond, this is detected as failure and displayed as a flashing light at the top of the unit at the corresponding pin number. A 16-position rotary switch, at the side of the unit, allows one to dial up any particular pin and, when very short pulses occur, a built-in pulse stretching circuit indicates this high-frequency action through a uniform flashing rate. The Faultrack 200 also has a small jack that can be connected to a 175 mm extension probe which takes over the display, regardless of the pin number dialed, and can be used to probe on adjacent circuit pins to make sure that the pulse or square-wave signal exists at that point. This feature helps the test engineer to detect a broken path or cold solder joint between adjacent ICs. An automatic power-seeking circuit is included, but it is also possible to use external power leads.

Disadvantages:

* One of the limitations of the Faultrack 200 is that it will not test the ECL IC family and will only test CMOS ICs at lower frequencies.
* The greatest drawback of this device is that it require a good reference IC at all times.

If the test engineer wants to do a relatively large amount of digital IC testing, the Faultrack 200 will soon pay for itself in time saved.

2.2.1 Basic method of IC testing with the Faultrack 200:

At the start, the test engineer has to know the type number of the suspected IC and must have one that he knows is working properly to use as a reference. If all active inputs are toggling as indicated by the flashing lights, he then make the decision as to whether the IC passes or fails. If it passes, he move the test clip to the next IC and plug in another reference IC. The next IC in this case is not necessarily the adjacent one, but the one that follows it in the logic sequence according to the manufacturer's diagram. If the active inputs are not toggling properly, he has to determine if the preceding IC might have a stuck pin, and the IC under test is therefore not receiving the proper input. If the preceding IC has been tested correctly, then he will suspect an open circuit between the two ICs. The manufacturer of the Faultrack 200 provides a series of flow charts, for a more thorough analysis of the various logic problems that can occur. From the flowchart, the Faultrack 200 comes in handy when the test personal are checking out large numbers of digital ICs.

BASIC METHOD OF IC TESTING WITH THE FAULTRACK 200

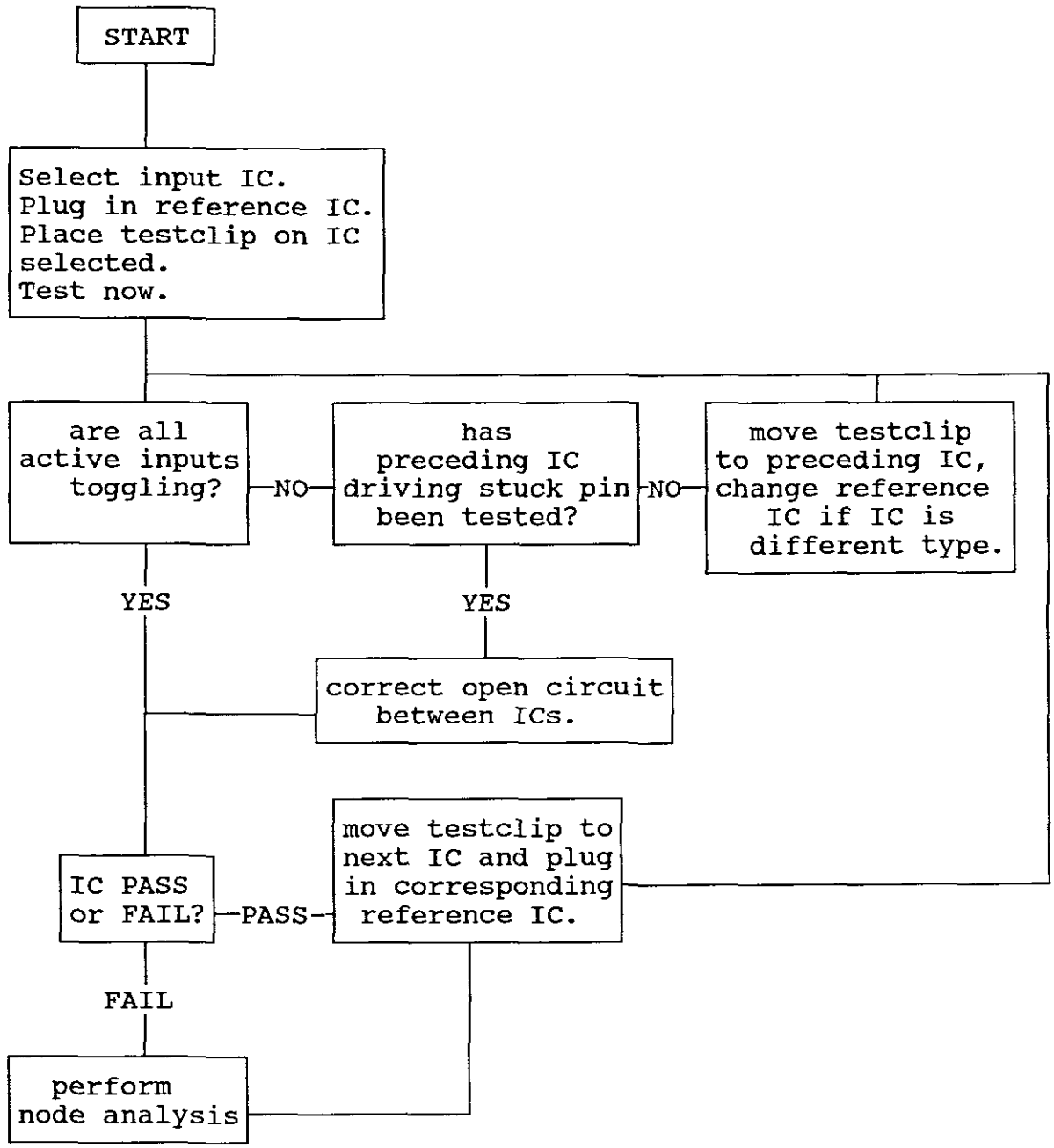


fig.2.2.1

2.3 A PORTABLE LOGIC CARD TESTER:

In many complex digital equipment, large numbers of plug-in PC cards are used and much of the troubleshooting consists of changing these cards until the defect disappears. The major disadvantage of this approach is that it requires a large quantity of spare PC cards and in addition, some types of defects can ruin every PC card plugged into the particular socket.

One solution to this problem is to use a portable PC card tester like the Datatester 2000. This unit is typical of the logic testers that field service engineers carry with them. It is contained in a sturdy aluminum case of a size suitable for air travel. The PC board under test is plugged into a program module which is specially designed for the type of PC cards that are used. This program module is available with a variety of PC board connectors and connects the pins of these PC plug-in connectors to the two matrix boards. The actual interconnections are established by shorting pins that are inserted in each of the two matrix assemblies according to prepunched templates. A particular program module with its PC plug-in connectors will be furnished by the equipment manufacturer for a particular computer, data set, or similar digital equipment. Different templates and different arrangements of shorting pins on the matrix board are required for each type of PC board to be tested.

In order to use a tester of this type, the test engineer first has to have the appropriate test module, equipped with the right connectors and wired to them. Next, he should have a template or a list of connecting pin layouts for the matrix. Once he has these two steps completed, he can proceed in a variety of different ways. If he has another PC board of the same type as the one to be tested and if he knows that that PC board works properly, he can plug it in first and use the probe to check all of the output points. The test engineer record each of the outputs. The probe contains a four-digit LED display, an indicator to show the end of test, and another indicator to show logic level problems. The four-digit display shows count data representing the number of transitions above the preset threshold level at a particular probe point. The test probe can be used on a single cycle where one complete test sequence is presented each time the start-test push button is pressed. It can recycle the test so that the test sequence is automatically restarted after a two-second readout. It is also possible to use an external pulse generator instead of the internal one that can be controlled by the front panel controls.

The test data of the circuit board known to be good can be recorded and used to repeat the test on the suspected circuit board. The output point at which there is a difference in reading can then be found, and from there the defective IC can be located. If only the suspected PC board is available, the testing may take a little longer, because the PC board have to be analyzed carefully to determine what the output at each output pin should be.

It is also possible to test the PC board, IC by IC, by means of the test probe, but that of course, will be much more time consuming than the comparison method. The tester itself contains its own pulse generator and buffer as well as a number of indicators. Four separate power supplies are included that can supply a variety of voltages up to 30 volts DC, positive or negative . A separate indicator is provided for each power supply voltage which is illuminated when an overload occurs. This tells the test engineer that the identified power supply may be shorted to ground or at least is drawing excessive current. The built-in pulse generator provides two independent two-phase clocks or one four-phase clock, a variety of reset signals, and a variety of test patterns that can be exercised from 40 independent lines. It may take a while to learn how to operate this type of logic tester but, once familiar with its use, it saves a lot of time in testing PC boards and is extremely efficient, particularly where large quantities of similar PC cards are used.

2.4 FACTRON TESTERS:

FACTRON produces a variety of test machines which provide a large range complement of highly sophisticated test capabilities within the electronics factory. In general, all FACTRON testers perform the following functions:

* Write or simulate test procedures.
* Connect the appropriate equipment to the PC board.
* Apply stimuli and perform measurement sequences.
* Determine whether the circuit(s) or component(s) are OK.
* Perform fault isolation and report a fault location.
* Repeat this for every circuit on the board.

2.5 PST100 Pre-Screening Test System:

With the cost of ATE soaring as suppliers add more and more facilities into their functional and in circuit test systems, users and prospective users are looking much more seriously at methods to improve the quality of their manufacturing processes, ie increase first time yields, and at the same time reducing the cost of the test. Ongoing cost of test for today's complex products based on conventional systems is becoming prohibitively high. Even large manufacturing companies which, in the past, have supported substantial test engineering teams, can no longer justify the investment cost in program development. For functional testing this can be measured in months, and for in-circuit testing the problem is equally serious because the suppliers cannot develop adequate software models as fast as new microprocessors, support chips and custom VLSI devices are appearing. Since the largest category of faults at first time board testing is gross manufacturing errors, there clearly is a need for pre-screening to eliminate them before other forms of product testing take place. Other forms of testing, though not necessarily based on ATE, will exist to ensure that the product is fault free and performs satisfactorily prior to shipment.

The message is summarised in two points:

* By far the largest percentage of all faults at first time testing are gross manufacturing errors.
* Cost of programs and fixtures over a five year life of an ATE can exceed the initial purchase price many times over.

The Olivetti Tecnost PST100 pre-screening system was designed to address these problems. This system uses the in-circuit test technique, integrated with revolutionary concepts of autolearning, and progressive programming for upgrading test sophistication. In order to be effective as a pre-screener, it offers the following important features.
It is:

* able to detect and diagnose gross manufacturing defects;
* effective on all component technologies;
* not limited by component or product complexity;
* quick and easy to program;
* provides simple low cost fixturing.

In a high volume manufacturing plant it can be used in two ways:

* in pre-production pilot runs to sort out process errors prior to main production;

In small-to-medium scale production:

* as a low cost solution where higher performance test systems cannot be economically justified.

For first time ATE users:

* as a logical first step to complement and enhance manual or semi-automatic test and inspection procedures.

3.0 TECHNIQUES OF ADVANCED IN-CIRCUIT TESTING

Components in free space are much easier to test than interconnected components. This is due solely to the fact that with free space components, there is easier access to all inputs and outputs. When however, components are interconnected, their inputs and outputs are connected to other components, thereby complicating the problem of access. Because of this, a manual PC test will always view the board as a single, functioning unit. When a problem is detected, a series of logical and well thoughtout steps must be followed in order to effectively locate any problem.

3.1 MANUAL TESTING:

Manual testing of a PC board requires the following information:

* PC board theory of operation.
* PC board schematic and parts list.
* Well thoughtout test diagnostics/procedures.
* Functional "hot mock-up" of the system for which the PC board is targeted.
* Appropriate type and quantity of measurement equipment.
* Ability to make electrical connections efficiently.
* Smart technician or technicians.
* Lots of time.

Manual testing can be a "bear" of a task and one which is not cost effective with respect to the manufacturers quality and throughput requirements.

3.2 AUTOMATIC TEST EQUIPMENT:

Automatic test equipment is the common sense substitute for manual testing. The ATE will supply both the hardware and the software intelligence to solve the testing problems in a systematic and efficient manner. There are two systematic approaches to ATE's, in-circuit and functional. Each technique has an application and solves a specific problem. The terms in-circuit and functional are used quite extensively throughout all ATE literature.

3.2.1 In-circuit Testing:

That type of testing which views the printed circuit board as a "bunch of parts". It attempts to test each individual part as if it were all alone or standing in free space.

Characteristics:

* Rapid program development and debugging.
* Good diagnostics (fault isolation).
* Conventional in circuit = catastrophic fault coverage.
* High performance in circuit = catastrophic fault coverage + component dynamic problem.
* Capable of locating a multitude of errors in single test pass.

3.2.2 Functional Testing:

That type of testing which views the printed circuit board as a single functioning unit. It attempts to test the entire board in a environment which closely emulates that system for which it was targeted. But again, it does not look at the board as a bunch of parts.

Characteristics:

* Much slower program development and debug.
* Extremely good diagnostics (fault isolation) via "guided probe".
* Positioned to cover all problems not covered by the conventional and/or high performance in circuit tester.
* Capable of locating one or a few errors in single test pass.

3.3 BED OF NAILS:

The most advanced ATE's make use of the "BED OF NAILS" technique. The in circuit tester examines the PC board as a bunch of parts. This is the only way a tester could access every electrical network on the PC card at the same time.

A bed of nails fixture is a special plug which connects the PC board to the in circuit tester. An electrical plug has two or three prongs, while a bed of nails fixture has many more prongs. In fact, a typical in circuit fixture can have hundreds or even thousands of prongs. Generally speaking one prong per network is the rule. The nails are usually spring loaded probes with tips that resemble miniature meat tenderizers or tulips. These unusual designs help to form better electrical contact with the solder side of the PC board. Bed of nails fixture is custom built to match the users PC board design and network layout.

The position of each nail must be selected with regard to both the schematic and the solder side network. The bed of nails fixture is a box with a top side rubber gasket that forms an airtight seal with the PC card in position. During testing, while using this technique, vacuum is brought into the tester and piped up to the fixture. The airtight space inside the fixture box is evacuated, and the PC card is gently, but firmly, brought down onto the spring loaded probe field. The multitude of probe tips then simultaneously cut through any layer of contaminants on the PC solder side creating a high reliable electrical contact.

3.3.1 Pincheck:

The premise of "pincheck" is that if current can be detect on a nail, then it must be making electrical contact. By applying positive voltage to both power and ground, the voltage difference between power and ground is zero. Then there exists a net voltage difference with respect to the scanned fixture point. When the point is scanned, a high resistance is connected from each network to ground in succession, thereby creating minute currents that flow into the nails. The input impedance to the driver/sensor acts as a voltage divider to ground.

A good tester "pincheck" capability is characterized by a very high input impedance, typically greater than 400KΩ. When currents are not detected, the tester makes the assumption that the probe tip is not making contact and will abort the balance of the test and then notify the operator of the fixture contact point. The benefit of course, is that a faulty nail contact has being found, rather than indicting a good component later on in the test.

3.3.2 Shorts test:

After passing PINCHECK, the tester will check the PC cards for any network shorts. Network shorts are caused by two things:

* solder bridges or
* mechanical problems.

Shorts are low-resistance paths, while opens are high-resistance paths. The concept of "threshold resistance" is important here. If we say that every path ≤ 10Ω is a short, and every path > 10Ω is an open, then 10Ω is called the threshold. By varying the threshold resistance, we can focus on specific levels of resistance shorts on the PC. Indeed a very flexible and useful testing concept!

In determining whether a short exists on any given pair of networks, the tester must be able to individually control which pairs of nail probes it will be measuring simultaneously. With a known "good" PC board testing on the bed of nails fixture and a threshold resistance set, the tester begins to learn the location of any shorts. Pretend a PC board has 256 networks. Node (1) is checked against node (2); (1) against (3); (1) against (4);...(1) against (256); then node (2) against (3); (2) against (4) ... (2) against (256); then (3) against (4) and so on; finally (255) against (256) and the learning is complete.

One way to visualize a test for shorts is with a square. Using the same 256 network PC card. Let the square be 256 x 256 cells. The diagonal of the square is always (1); that is, each node is shorted to itself. Also, the upper triangular portion of the square is filled with ones or zeros. This is because the lower triangular portion is redundant with the upper triangular portion; ((1) to (2) is the same as (2) to (1)). If the whole square were filled, it would be 256 x 256. But only the upper triangular half was filled, so we have (256 x 256)/2. Knowing the diagonal is always (1), we have [(256 x 256)/2] - 256.

EXAMPLE:

For a number of 10 nodes on the PC board:

$$\text{The number of learn operations} = \frac{(10 \times 10)}{2} - 10$$

$$= 40$$

However, FACTRON has developed a shorts scanning system which drastically reduces by orders of magnitude, the number of learn operations during the cause of a shorts test. Because of this, the in circuit testers can perform this learn and measure scan in a matter of seconds!

A well-known law of physics states: "Whatever one try to measure something, one always interfere with the thing you are trying to measure", or another well-known law of Murphydom states: "Whatever can go wrong, will go wrong."

3.3.3 Disadvantages of bed of nails technique:

The ingenious method of bed of nails fixturing can also work against the user. In reality, a fixture is a bunch of metal connected to a spaghetti plate of wire (which is also more metal). The metal has resistance, capacitance, inductance and antenna-like broadcasting qualities. Mysterious electrical glitches and/or stray and unwanted signals can appear within the in circuit test. "Noise" is the key word here. Elimination and/or suppression of noise is the goal, because noise can cause erroneous failures, hinder test debugging and can only lower the quality of test.

When choosing automatic test equipment, make sure that the ATE manufacturer has included special fixturing details which reduce and/or eliminate noise, such as:

* Twisted pairs of wire within the fixture.
* Heavy grounding planes.
* Coaxial coupling cable to the receiver for instruments.

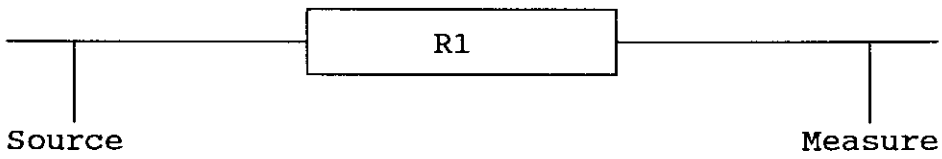
The faster and more intelligently the test procedure, noise will become more apparent and due consideration is warranted.

What sets the in circuit tester apart from all other types of testers? It is the fact that it views the printed circuit board as individual parts, and always attempts to isolate these parts as if they were in free space during testing.

3.4 TESTING COMPONENTS:

3.4.1 One resistor:

Let's look at the problem of testing a simple resistor in free space. The resistor has two terminals and, therefore, requires a two terminal measurement:



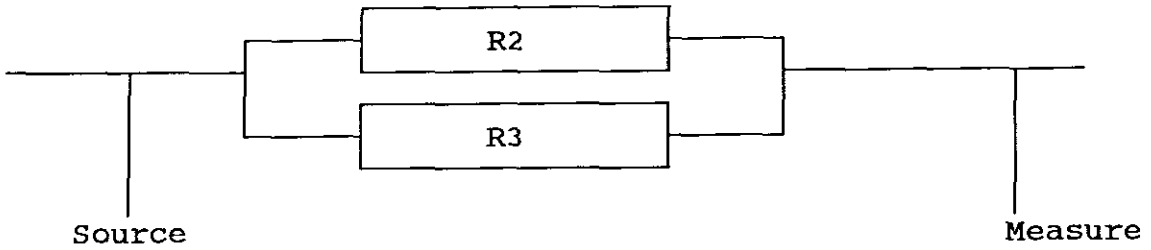
Using Ohm's law:..... Voltage across the resistor is proportional to the current through the resistor;

$$R = V/I$$

An in circuit tester would "source" a known current and "measure" a voltage. The ratio of voltage to current is the resistance.

3.4.2 Two resistors:

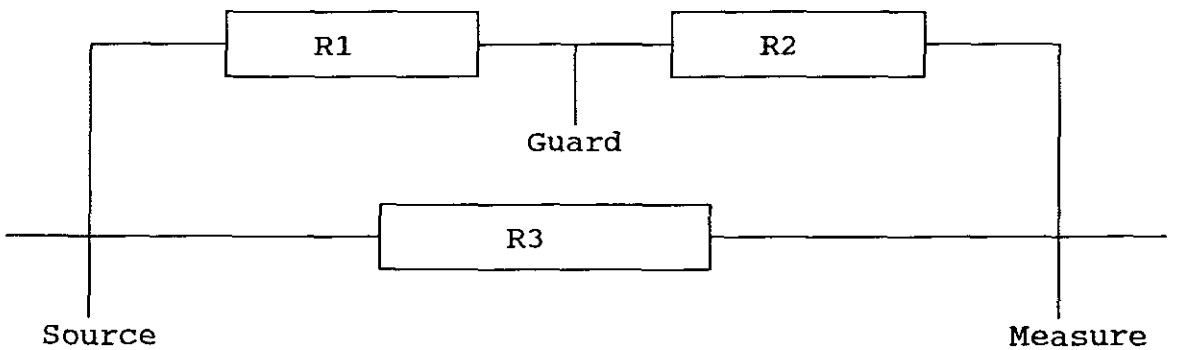
In this situation, the source current would flow through both resistors.



The voltage measured would result from the parallel combination of both resistors. In this example, the tester must view these resistors as one component with a value equal to the parallel combination of both. This is a limitation of all in-circuit testers.

3.4.3 Three resistors:

Here are two resistors in series with each other but in parallel with a third resister.



Using the source and measure concept as previously described, a resistance which would be equal to the series combinations of R1 and R2 in parallel with R3 will be measured. The key here is to stop the current from flowing through the path R1 + R2. If this happened, all the current will be forced through the shunt path R3 and the measured voltage would correspond to R3 only. This is called "Guarding."

"Guarding" is a in circuit testing technique in which the in circuit tester isolates the components. A guard point is nothing more than a forced ground. If the point between R1 and R2 were forced to ground, then because of the internal measurement circuitry of the tester, the current in path R1 + R2 would be effectively shut off, and thereby isolate R3 in circuit. But this isn't as simple as it sounds. The fact is that the guard point is not a perfect ground. Few things in life ever are perfect. Some current does shunt through R1 + R2. In fact some current does leak through all the connected wires. Draining off tiny bits of current causes error in the measurement scheme.

This error can be comparatively very small, or it can be comparatively very large, and therefore a "guard ratio" will be used.

The guard ratio is the value of the part when measuring (R3) over the parallel combination of the parallel resistance (R1//R2). or;

$$\text{GUARD RATIO} = \frac{R3}{(R1 \,//\, R2)}$$

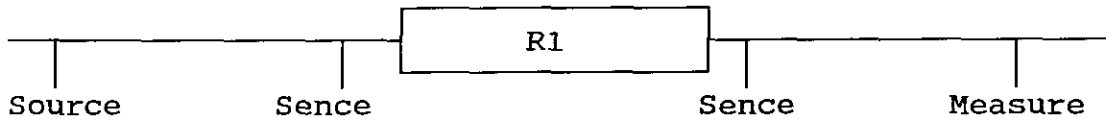
As the guard ratio becomes small (10 or less), then R1 // R 2 becomes very large, making R1 and R2 both sizable resistors. This would tend to imply that a small current would flow down the R1 + R2 path naturally and irrespective of use of the guarding point. Therefore, small guard ratios are circuits which are easier to test and easier to obtain results. As the guard ratio becomes large (say 1000 or more), then R1 // R2 becomes very small or R1 and R2 are both small resistors. This would tend to imply that a large current would flow down the R1 + R2 path naturally, regardless of the guarding point. It is more difficult to obtain accurate test results with large guard ratios.

3.4.4 Other solutions:

Introducing the fourth wire. Sense is a concept which says that the tester are sensing the actual voltage (or current) at the actual point in question. Sense feeds back the actual voltage or current information into the source/measurement system to compensate for the errors found within the physical wires. Remember, the metal offers resistance, capacitance and inductance. From this point on, let's call these electrical elements "residuals". There are two common ways to use fourth wires: 4-WIRE KELVIN and 4-WIRE GUARD sense.

3.4.4.1 4-Wire Kelvin testing:

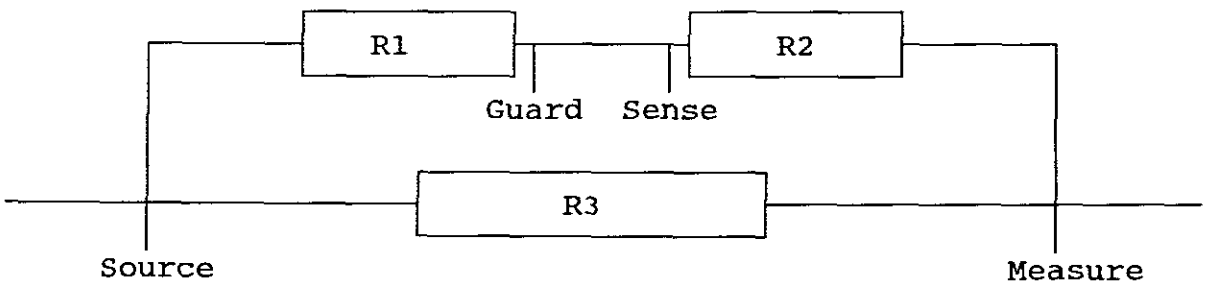
Both the source and the measure are being "sensed" to compensate for the residuals and, therefore increasing the accuracy of the 2-wire measurement.



The most appropriate application of 4-wire Kelvin testing is in very accurate measurements on low-value impedances.

3.4.4.2 4-Wire guard testing:

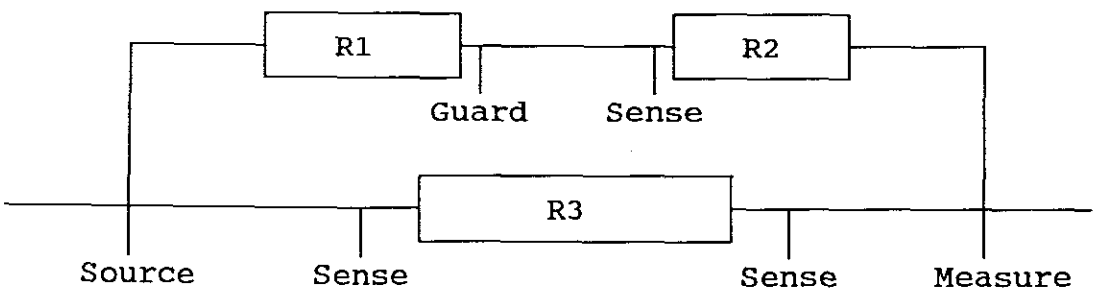
For parallel circuits;



In this case, the guard point is sensed for the actual voltage reading. When the guard ratio becomes large, the nonground voltage difference at this point becomes very significant.

3.4.4.3 6-Wire measurement scheme:

For more accuracy and residual sensing the user can have a 6-wire testing.



Again, the sense technique is extended to each of the basic three wires, source, measurement, and guard.

3.5 TYPE OF CONFIGURATIONS:

The main question here would be ,"How does the prospective user knows what configuration must he uses, when and where?." Some manufacturers will provide that type of information. (FACTRON's in-circuit testers etc.)

The tester itself will:

* Recommend the correct configuration for the circuit under test.
* Recommend what hardware is available in the tester.
* Write the software test to make all the connections.
* Provide the correct wire scheme so that the fixture can be made.
* Do all the above automatically.

Generally speaking, in circuit testers address much more than just resistors and DC signals. In fact, each of the resistor boxes given in the previous examples can be replaced with a more generalized component called " complex impedance." Complex impedances are here associated with AC sources and measurements. Since an impedance can be described in terms of its root mean square (RMS) value, all the prior concepts relating to guard ratios and guarding can still be applied.

Analog measurement systems must offer the following capabilities and characteristics.
They must be able to:

* Perform 3-, 4- or 6-wire measurements automatically.
* Perform "quadrature" (will be discussed later...)
* Route and synchronize IEEE instruments onto the measurements bus.
* Perform hybrid (i.e., digital/analog) testing.
* Accommodate unpredictable steady-state conditions on PC board with an automatic wait time function.

(FACTRON offers all of the above features in its analog measurement systems.)

3.6 ADVANCED ANALOG TESTING FEATURES:

A testing mode is a way to perform a test. All testing is build on one overriding theorem: "Apply a known and controllable stimulus and... learn a response from a "known good" circuit".

There are two corollaries to this theorem:

(a) The known good circuit must be really known good!
(b) If the learned response from the known good circuit corresponds to the theoretical value, then great!

3.6.1 Quadrature:

Quadrature, mentioned earlier, is an interesting technique used to test analog components or analog networks. The concept is simple. First, provide a pure AC source to the input of an analog network to be tested. Then the output of the analog network is summed (internally in the tester) with a 90-degree, phase-shifted version of the original AC source. The sum is presented to a low-pass filter, and the output of the filter is stored. The results are the real and reactive values of the components under test. But it's not so simple after all.

What the tester has just done in this procedure is to learn the stimulus (response) of the analog network under test, and store the response in terms of its real and imaginary components. From this information, the test engineer can get useful test data such as RMS and phase values.

The real benefit of quadrature is that it provides a testing method for certain analog networks which were not previously testable. Quadrature revolves its RMS measurements into their real and imaginary phasor components. Each phasor component is of a lesser magnitude than the total RMS phasor itself. The measurement system can therefore, scale itself to a lower (and more accurate) range. Quadrature seems to be a good testing approach in this case, while other approaches probably will fail.

3.6.2 RC-networks:

Perhaps the most common type of analog, in circuit network is the "tank"... the parallel RC network! And, recalling Mr. Murphy, this is also one of the most troublesome types of analog network to test.

Why is the tank such an unruly beast? Two reasons;

(a) Many tanks have very high-resonant frequencies. (the value of 1/RC).

(b) Wrong values for tanks can cause the tester to actually run inefficiently.

In testing a tank, the tester expects to see a very specific value for 1/RC. Knowing this value, the tester applies a stimulus and waits a designated period of time (which is tied to some integer multiple of 1/RC). After waiting, the tester assumes that the tank has attained close to its maximum charge (or stored energy), and then strobes a measurement.

Suppose a tank were the wrong tank. And this particular tank has a value for 1/RC, which is orders of magnitude smaller than the expected value of 1/RC (the one from the parts list). This wrong tank will reach its maximum charge much sooner than expected, and the tester could then strobe its measurement much sooner than expected. If the tester could detect this, then it would save time especially if there were a large number of similar tanks on the PC board under test.

3.6.3 Automatic wait time:

With automatic wait time, the tester can monitor the change in charge on the tank, and by interpreting the change in current per time, it can determine when it was close to "steady state" on the tank. In a sense, the tester is learning some response from the PC board under test. It's also accommodating the production error to both find the fault and optimize the tester throughput.

3.7 DIGITAL TESTING:

When trying to test a fully assembled PC board, complete with digital components, three possible techniques can be used.

(a) Take each digital component out and test it individually in a component tester (Not very practical).

(b) Try to figure out how to stimulate each digital device from the PC board edge or some other remote input point. This is actually what a functional tester does, and although valid for its application it is clearly not within the framework of the in circuit test philosophy.

(c) Overdrive (or back drive) each device network as if the connected components were not even there (Can be dangerous)!

Generally speaking, the output/input of any gate is really the output/input of a transistor configuration. Transistor outputs have very low impedance compared to transistor inputs which have a very high impedance. When an in circuit tester back drives into a network, it is really sourcing or sinking the current. Most of this current will drive toward the low impedance (the output transistor) the gate which is being back driven. Since the output transistor is not designed to handle this over driving current, it simply heats up. This is because the over driving current is taking a path right through the base-collector or the base-emitter junction, which is not protected by a current limiting resistor.

The temperature of the transistor output junction increases when it is back driven. The temperature threshold of the transistor actually saves the test engineer from a catastrophe. Both theory and practice demonstrated time and time again, that as long as the temperature threshold of the transistor is not violated, the component will not be damaged. The actual value of the temperature threshold is really a function of what the transistor is made out of, but 120 degrees centigrade has become the accepted number for silicon transistors. The art of back driving is really a game of heat transfer (heat rising and heat cooling within the transistor junction). There are three techniques used by in circuit testers in the game of heat transfer:

(a) Back driving very fast, so that the test is over before any significant heat can build up within the junction.
(b) Current limiting, allowing the in circuit driver to source or sink only what is necessary to force the network.
(c) Programmable, back driving duty cycle (PROTECTOR).

3.7.1 Protector:

For small-scale integration (SSI) to medium scale integration (MSI) digital devices, the speed and current limiting methods work fine. This is due primarily to the fact that the back driving burst is relatively short lived preventing heat from accumulating appreciably.

However, large-scale integration (LSI) devices require much longer bursts or tests to fully exercise their functions. Not only are the bursts longer, but there are separate bursts to test different LSI functions. Suppose a heat transfer game can be played, in which the ratio of time spent bursting to the time spent not bursting can be controlled. Both the device specifications and the quality assurance department can dictate the amount of back drive exposure the devices will receive. By playing this heat game, the heat flow into and heat dissipation out of the junction can be controlled so that it never violate the threshold temperature of each device. In other words "thermal dynamic equilibrium". (FACTRON's PROTECTOR allows duty-cycle programming from 0-100% over a range of 0 - 1,3 seconds.)

Like everything else, nothing is perfect. The vision of a "NAND" gate sitting in the middle of some nice circuitry is much too simply. In real life the in circuit testers encounter circuits which contain feedback loops, or Buses.

Feedback loops are circuits which feed their outputs back to earlier stages of logic so that the outputs affect the inputs of the circuitry.

Buses are groups of wires which share more than one device. Some buses allow the devices to be individually turned off and on, permitting only one device to talk on the bus at once. But this is not always the situation.

3.7.2 Testing "Loops":

Consider the classic example of the J-K type flip-flop which is loop connected to a NAND gate from Q to the NAND gate input. The NAND gate output feeds the clock input of the J-K type flip-flop. A problem occurs when the flip-flop changes state, or logically speaking, both Q and not-Q flip their states. If Q flips its state, then so does the NAND gate input. If the input to the NAND gate changes, then this in turn can, and frequently does, change the NAND gate output.

A J-K TYPE FLIP-FLOP IN CLOCK FEEDBACK WITH A NAND GATE:

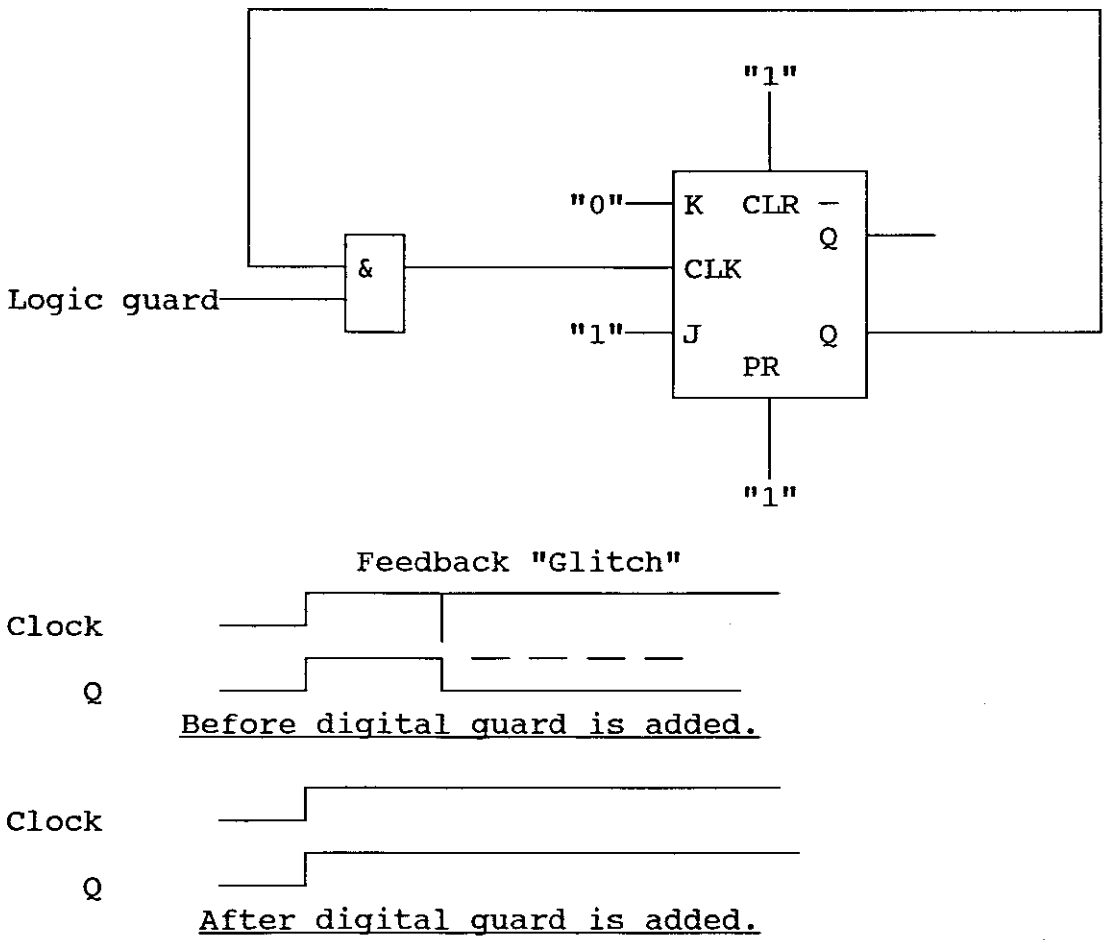


fig.3.7.2

Of course, the tester driver on the NAND gates output is doing its very best to keep that network in the correct state. But, if the NAND gate decides to change its preferred output state, a transient voltage can develop on this network for a short period of time. Some refer to this voltage as a glitch.

The clock input of the flip-flop doesn't really care that the glitch occurred for a short period of time. It cares about the edge (or change of voltage) on the glitch. So, from the flip-flop's perspective, it just saw another clock edge! An unwanted clock edge and an erroneous test with false results...

The key here is the preferred state of the NAND gate. Suppose the NAND gate is kept stable during the flip-flop test?

Applying a logic zero on the other NAND input, the NAND gate can be kept in a constant preferred output state of logic. The guard is the instrument which isolates the analog device under test by grounding (or breaking) feedback paths within the analog networks.

3.7.3 Digital guard:

The digital guard is a tester driver point which is programmed to maintain a solid, static logic level (either logic zero or one) on a network during the duration of a test burst. FACTRON'S tester, drivers can both source and sink solid currents for both back driving and guarding. Some *specifications are:*

Source up to 500 mA.
Sink up to 300 mA.

3.7.4 Bus testing:

A bus designed for testability allows the tester to selectively "enable" or "disable" any device on that particular bus. The in circuit tester is designed for the sole purpose of keeping one device active at a time for testing by means of driving logic zero's and logic one's throughout the enables on the bus.

3.7.5 Truth tables:

All gates have truth tables, and the tester is only interested in whether the network ever reached the correct logic state. A logic low might represent all voltages which are less than or equal to 0.8V, while a logic high might represent a voltage which is greater than or equal to 2.7V. Generally, these specific voltage thresholds should be programmable within the tester, and are intended to accommodate a wide range of logic technology families.

3.7.6 Static digital testing:

A truth table test is a "static digital test". The fault coverage of a static digital test is limited to catastrophic faults only!
Catastrophic digital failures occur when:

* Parts are missing,
* Parts are installed backwards,
* Parts are partially dead or,
* Parts are completely dead.

But there's more to it. There is a whole classification of faults above and beyond the catastrophic level referred to as component dynamic faults. For every fault the test engineer don't catch at the in circuit tester level, he has to catch the fault at some later level of testing (a much more expensive proposition).

Each one of the categories of component dynamic faults is a criterion by which incoming devices can be judged. So, now the question arises: How do component dynamic faults get into a factory? The first and most obvious answer is the front door, or the back door (depending upon where the receiving department is). The fact is, without thorough incoming inspection, the manufacturing process may have to suffer the consequences of accepting digital devices with component dynamic faults or even devices with borderline component dynamic faults.

The second point, are the possibility of devices developing borderline component dynamic faults during the hot soldering process. Component dynamic faults are more difficult to catch than component catastrophic faults. The tester must simply be more powerful and it must contain the right stuff!

The "big boys" will call the right stuff;

- A State-of-the Art Timing Generation and Pattern Control.
  - * Accurate Timing/Formatting.
  - * High Resolution/Accuracy.
  - * Sequence Processor.
  - * High-speed Driver/Sensors.
  - * Flexible "RAM-Behind-the-Pins Architecture.

- Test Driver Support Features.
  - * Unit Under Test (UUT) Synchronization Through Channels.
  - * Trigger channels through the channels.
  - * Clocking through the channels.

- Debugging capability.
  - * Debug panel.
  - * Debug software.
  - * A flexible pin design.

- Fault isolation facilities.
  - * Bus diagnostics facilities.
  - * Fault isolation software.

3.7.7 Putting the "Ram behind the pins":

A pin is sometimes used to describe a tester, driver/sensor point. It's the pin which performs the useful test work of an in circuit tester. But what's behind the pin is the most important with respect to just how useful that work may be. Putting memory (RAM) behind the pin is the key to tester pin intelligence. RAM backed pins have two features which are interrelated: one is RAM depth and the other is RAM configuration.

Factron offers two maximum RAM configurations which are software selectable:

* 4K by 4 (also called parallel mode).
* 16K by 1 (also called data mode).

The 4K by 4 parallel mode is designed to accommodate a sequence processor and real time data compression. The 16K by 1 data mode is designed to accommodate serial initialization and testing of level sensitive scanning devices (LSSD). LSSD's are series gate arrays which allow internal initialization by providing serial bit stream input/output ports. Typically, these devices require very long initializing patterns and that's the reason for 16K.

3.8 TIMING GENERATOR:

This is the heart of the machine which will detect and capture the spectre of the component dynamic faults. The best timing generators in the world are found in functional testers. The Factron allows simultaneous bursting on all dynamic pins in its tester. This allow the tester to broadside the device under test. In other words, the device is being tested with all of its ports stimulated and monitored simultaneously. This can only be a more realistic test. Factron makes the fastest in circuit testers on the market today, ten million patterns per second. In order to locate a component dynamic fault, the device must be test as realistically as possible. The device must be test at or near the way it is intended to be used and at or near the way it is specified in its data sheet.

The marriage of timing and formatting provides the vehicle by which the user can realistically stimulate and measure the device under test.

The heart of the timing generator is the master clock. Since the timing generator produces groups of synchronous timing signals, it would by convenient to control these signals with one, very precise clock. The "time unit" is the smallest increment of the master clock signal. Factron's timing generator uses a time unit with the following specifications:

* Programmable to a minimum of 10 ns.
* Programming resolution as small as 200 ps.
* Accuracy is 0.8% of the programmed time unit.

The master clock drives all other timing generator signals such as the event frame, event pulse, etc.

The smallest unit of the burst is the Test step, Test vector, or Event frame. These three terms are all synonyms for the same concept. Factron offers up to eight definable event frames. These frames can be programmed in any sequence and will change on the fly. They can even be programmed in master clock increments. The event frame acts as the master template for the test step which may be stimulating and/or measuring a digital signal. Within the boundaries of the event frame comes the need to perform very specific operations. And this is where formatting really helps. This function can:

* Apply new data.
* Toggle data.
* Invert data.
* Measure data in an instant.
* Measure data during a window of time.
* Tri-state networks.
* etc.

Factron offers up to eight event pulses for each and every event frame for a total of up to 64 different, definable vector templates which, again, can all change. Each event pulse can also be programmed in master clock increments for surgical precision in the quest for component dynamic faults. With the advent of faster, smarter and more sophisticated devices to be tested in-circuit, there is a growing need for the tester to be able to maintain synchronization with the component under test. Take for example, a microprocessor which is driven by an on board clock "a crystal oscillator." The crystal oscillator produces a clock which is 10 MHz. This clock not only keeps the microprocessor alive, but also serves as the actual clock when the board is plugged into the system. Let's complicate this example by adding that the crystal oscillator circuit has not been designed for testability so there exists no easy way to "kill" the clock. Factron offers on-board synchronization of up to 10 MHz through its test channels. Factron can also provide 50 MHz of synchronization via its test receiver input, but this one is hard wired.

The 74LS163 4-bit counter which "Harry" was so kind to leave uninitializable will probably cause much grief and pain to three departments, Design Engineering, Test Engineering, and Accounting. Unless, of course, Test Engineering owns a Factron tester with its powerful trigger channel feature. The real problem is that the counter cannot be initialized before the test begins. Ideally, the test engineer (TE) would want to put the counter into a known state and then begin the burst. He could learn and/or predict the outputs by using various methods at his disposal. The trigger channels give the tester the vehicle to monitor the outputs of the counter, and then branch (in real time) to the beginning of the actual test upon detection of the predetermined, initial state. This predetermined, initial state is set by the TE in software. The concept of monitoring on-board states, followed by branch to test, is a general concept which can be extended to a multitude of devices and device situations. Last, but not least, is the fact that the three groups of 16 trigger channels in the Factron testers are through the test channels. All triggers are set up in software only, and there is no need to add additional fixture wiring to account for this capability.

Referring to of course, is the fact that dynamic devices require timing to maintain their internal memories and states. Dynamic random access memory (DRAM) is only one example of this and users are starting to see more and more microprocessors with this test requirement. Conventional in circuit testers worked around this problem by externally adding clocking circuits to the fixture. It works but is not convenient, efficient and as cost effective as the alternative.

3.8.1 Clocking through the test channels:

Factron offers the capability to provide programmable clocks on all its dynamic pins. Each clock can be programmed up to 10 MHz with no hardware involved.

A little known fact is that a large portion of what a TE does, is to kill bugs (Test bugs). When debugging a test program, a variety of things can go wrong:

* Maybe the fixture is faulty.
* Maybe the "known good" board is not so "known good".
* Maybe the software kit is faulty.
* Maybe the data base is faulty.
* Maybe the device models are faulty.

And last but not least...
OK... maybe noise is the problem.

To fully appreciate what is involved in debugging a test program, the user should look at what is required to create a test program.

3.9 REQUIREMENTS FOR A TEST PROGRAM:

Creation of a test program involve various stages of software and hardware development. This includes :

* Schematic capture.
* Automatic program generation (APG).
* Creation of the test fixture.
* Debug of the test software.
* Qualification of a large sample of boards.

3.9.1 Schematic capture:

Boards are composed of parts and networks. In circuit testers look at the board as a bunch of parts and networks. Schematics represent these parts and networks to the tester. Therefore, the user must feed the data associated with the schematic into the tester. This can be accomplished in one of two ways:

* Manually (via a keyboard).
* Automatically (via a CAD system).

3.9.2 Component libraries:

Electrical devices perform very specific operations (functions). Analog devices have voltage versus current-time relationships where digital devices have truth tables, state tables and dynamic characteristics. In software, one can represent these devices and their functions. The ATE company should supply with the tester a large, comprehensive library. The books in this library are the device models and the user should be able to both use and modify these models for his own custom applications. If the device model does not exist within the standard library, then the tester manufacturer should supply the customer with the ability to easily develop these missing models. The ATE company should supply the customer with the link to " off-the-shell" simulators which can greatly help in this model creation. Again, the simplicity of viewing the board as a bunch of parts allows the very efficient process of in circuit automatic program generation (APG).

The primary functions of APG are as follows.

* Merge the schematic data and the library models.
* Account for all fixture wiring.
* Assign all dynamic nodes perfectly.
* Assign all logical guards.
* Generate the correct code in the correct order of testing.

3.10 DEBUGGING:

Let's assume that,
* The fixture wiring is correct.
* The data base is correct.
* The models are correct.

What's left? The guards!

A logical guard, is a guard which can usually be predicted by the APG. It's usually some feedback path or some serial path onto the device under test. Or, it can be some bus circuit or combination there of. But it's logical it's somehow networked back to the circuit under test.

A "noise guard" is not a logical guard. It cannot be predicted by the APG and usually, cannot be predicted by the test programmer. The noise guard can be due to one or all of the following:

Fixture intervention:
* The metal of the probes and wires adding R,L,C to the networks.
* Antenna crosstalk involved within the fixture wiring.

Thermal backdriving factors:
* Backdriving is an abnormal condition for a board and its components. Backdriving will cause voltage transients (or noise).

Poor PC blank construction:
* Although less common and harder to diagnose, it can be a cause of internal layer crosstalk and/or noise.
* Traces which are not designed for testability.

What this really means is that the traces are laid out with marginal susceptibility to noise interactions. The truth is that the board works fine as is, but when placed on the fixture and exposed to backdriving, noise becomes apparent.

Noise.

Symptom:	Unstable digital device test.
Diagnosis:	Noise.
Cure:	Place a guard in some nonlogical path with respect to the device under test.

Imagine the APG trying to predict the noise guard. It would have to have a mathematical model of all the parametrics involved within the text fixture and on the board itself. The computational time would far exceed the APG time, and it's not at all clear that this problem could be solved anyway. The best solution would be called efficient real-time debug. In other words, the test programmer (or engineer) takes a logical guess as to where to place a nonlogical guard. He places the noise guard and reruns the test routine. If it works, great! If not, then the next iteration, trial-and-error begins. The fact is that trial-and-error iterations of this type are much more effective than trying to math model predict the noise guards. It's interesting to note that even if the device test does work on the known good board, it still may not work and may be unstable when many other production known good boards are run through the same test. Let's call this production run the qualification stage.

PC boards are created on a "bell curve" of tolerance. The sample of one known good board will probably not account for the wider range of possibilities which will be encounter when the production are crank up. Therefore, noise guarding is a factor in both initial debug and the qualification stage.

Let's specifically leave debug for a short while and focus the attention on the variety of tester pin architectures which currently exist within the in circuit world. First, what is a pin architecture? The in circuit tester contains test points, or as some people call them, tester pins. Let's look at each one:
Simply, guard pin contention (GPC) is the biggest pitfall in a conventional and/or combinatorial multiplexed system.

Let's illustrate this pitfall by debugging a board on a tester which has a 4:16 conventional multiplexer.

The test engineer (TE) are debugging a digital device. The digital device is surrounded by other digital devices which all interact to enter into the backdriving test. The APG has already allocated logical guarding points which act to inhibit logical signal flow onto the device under test.

Although the board, the fixture, the logic guards, the model and the tester are all functioning correctly, the device test does not work. The first thing the TE now suspect is noise, so he proceed to add some digital guards around the area of the device under test. Now here's the problem. He is using 12 tester pins in a group of 48.

In other words, all the available tester pins for that device test are already in use. If he wish to add his noise guard, he will have to go into another multiplexed group to retrieve a wire. This will cause, at a minimum:

* A software change.
* A fixture wiring change.
* A fixture documentation change.
* A schematic documentation change.

And to top it off, if the change is severe enough, he may even have to return a portion of the APG!

All of these things take time and time is money. When fixtures and testers are tied up in debug, they are not available to test boards. When wires are swapped from other multiplexed groups, this can cause the additional debug of previously working tests:

The Rule: Don't debug that, which already works,
and
don't get caught off guard!

What is needed is the flexibility of a one-to-one system which the cost benefits of a multiplexed system. With FLEXPIN, the TE have a multiplexed 1:8 dynamic scheme. With S4FLEXPIN, the TE have a flexible one-to-one guarding scheme, or 8:8 that is, in each group of eight driver/sensors, one may be dynamic while the other seven are active for static latching (guarding). Therefore, seven eights of the entire machine is always available for guarding. The TE now have a giant pool of available test points for the addition of as many guards as he need.

FLEXPIN again eliminates guard pin contention, and the key here is efficient debug. The TE can now feel free to add as many guards into his device testing as he wishes in order to clean up and stabilize the tests. This extends to both the initial debug and the qualification stage. When a new guard point is added, the only impact is software and this is minimal.

Again, time is money, and one company like Factron can show the TE how FLEXPIN will save him 30-50% in program debug time. FLEXPIN allows efficient digital debug via its pin architecture. But the TE wants more. He want to be able to:

* Perform partial recompile.
* Have the ability to view his test signals conveniently.
* Have the ability to selectively place marker strobes, etc.

An efficient debug scenario will optimize the time spent in the debugging process, which is the most expensive portion of the ATE "cost of ownership".

When debugging the test program, the test engineer (TE) want to test some boards. But more than that, he wants to catch some board faults. Even more than that, he wants to pinpoint the exact locations of the faults.

3.11 Fault isolation:

Fault isolation is the ability of the tester, when it detects a fault, to precisely isolate the bad part or parts. There are two considerations, catching the parts which are bad, and not catching the parts which are good. Both considerations are equally as important. The former because this is what the job of a tester is, and the latter because of wastage and the always present possibility of further board damage when the board is repaired.

PINCHECK,3-,4-,6-wire guarding, and backdriving are all well designed methods of fault isolation. Each method attacks a specific group of board/fixture faults while ETCHPROBE gives the operator visibility to the open etches. One of the most challenging circuit types to test on an in circuit tester is the bus.

The bus is the type of circuit which connects many (digital) devices on the same line(s). The TE might remember that the key to testing the devices on the bus is the control given to the in circuit tester which enables each device to be selectively turned off and on, while other devices are being tested. And this is called guarding. There are two types of problems associated with a bus:

Output problems.
: Devices with leaky outputs (normally associated with internal diode problems).

Input problems.
: Devices with internal (soft) shorts which overdraw current from the bus.

3.12 TESTING FEATURES:

3.12.1 Flo-Finder:

FLO-FINDER is a standard feature on Factron's 730 tester. It works through the bed of nails fixture, and is designed to attack the fault isolation of the bus output problems. FLO-FINDER works in the following manner:

1. Before digital testing, each bus is individually tri-stated (all bus devices are disabled) and the tester tries to pull each bus line both high and low.
2. If the bus passes this test, then all digital testing proceeds as normal.

3. If the bus does not pass this test, then FLO-FINDER performs a test procedure which is unique to in circuit testers.

   3(a) When it gets to any device which was part of the faulty bus, it runs that device test to a pin-state which is opposite to the state in which the bus line failed.
   3(b) FLO-FINDER determines the fault by measuring the difference in the amount of current required to bring the bus line back to the opposite pin-state.
   3(c) BY viewing this "delta" current, FLO-FINDER can detect the specific presence of a faulty device.

FLO-FINDER is different from other commercial bus utilities for two reasons:

* It runs the device test dynamically: that is, if there exists a dynamic device on the bus (which requires keep-alive timing), FLO-FINDER will still be able to perform the test. This is opposed to a pure bus test which cannot address devices. Suppose we had a bus which contained more than one type of logic family? A bus test which just keyed on one value of this delta current might interpret a different logic family as a fault... an erroneous fault.
* FLO-FINDER can account for more than one type of logic family on the same bus. It can learn more than one value for the delta current.

3.12.2 Flo-Tracer:

FLO-TRACER is an optional feature on all of FACTRON's testers. FLO-TRACER works through two manually-guided probes and a footswitch. It's designed to attack the fault isolation problems associated with bus input problems and works as follows;
Suppose a faulty bus was detected by FLO-FINDER, yet each and every device on that faulty bus passed its test individually. As mentioned before, there are two types of bus problems: bus output problems and bus input problems. FLO-FINDER attacks the output problems first. Often it may be a input problem! The operator of the tester, in production, is told by the tester to probe/inject with the hand-held devices and activate with the footswitch. By methodically injecting/detecting current flow on the bus, the FLO-TRACER bus utility is able to pinpoint the location of the fault. FLO-TRACER is the only bus utility of its kind which is incorporated into an in circuit tester, when it comes to bus faults.

3.12.3 Analyst:

Analyst is an software package and a erroneous error filter. This is a standard package from most in circuit testers and it can be enabled or disabled by the tester programmer. With "analyst" enable and the test program running, analyst just collects all the tester detected errors, but no errors are printed. At the end of the program run, "analyst" looks at all the error data and data from the diagnostic utilities. "Analyst" then makes its decisions based on logical rules of device interactions using a probabilistic algorithm. It effectively filters what it believes to be erroneous faults.

4.0 SURFACE-MOUNT TESTING (FLUKE 9100)

4.1 AUTOMATED TESTING OF SURFACE-MOUNT BOARDS:

This chapter describe the steps Fluke took to test the 9100 Series surface-mount boards. It begins by explaining why surface-mount boards are difficult to test and how these problems can be solved through a combination of designing for testability and use of automated test procedures. It then explains the test configuration they are using at Fluke, the steps they went through to develop the automated test procedures, and the benefits they have with this approach.

Engineers and technicians who have tried to perform component-level troubleshooting on surface-mount boards know of the many problems that this new technology can present. In brief, problems range from difficulties in identifying the device in question (because many are too small to carry a label), difficulties in gaining access to it to test it (because the leads are inaccessible - or nonexistent). Fortunately, most of these problems can be eliminated through a combination of designing the boards for testability and using automated test procedures. At Fluke they have had to address these testability problems in manufacturing the 9100 Series Digital Test System. An automated tester and troubleshooter that includes eleven surface-mount boards. These boards are all very densely packed. The main board alone has over 400 components. Fluke solved the testability problems both by designing testability into the boards from the outset and by using automated test techniques. These involved setting up fully automated test and troubleshooting workstations, with the 9100 Series tester itself executing and controlling the test sequence. They also used robot-probers to eliminate the need for manual probing and an IBM PC AT to automate data management activities, eliminating most of the paperwork. The result was an extremely efficient and fully automated operation, from initial functional testing through component-level troubleshooting.

4.1.1 Why surface-mount boards are difficult to test:

Problems encountered in testing surface-mount boards typically fall into the following categories:

(a) Identification problems.
Many surface-mounted parts are too small to carry a label, and they may look so similar that it is hard to tell them apart. In addition, these devices are often packed so closely together on the board that there is no room to label them there either.

(b) Difficulty in finding unsoldered joints.
If a fault is due to an unsoldered joint, the troubleshooter may never find it, because pressure from the probe during the test may cause the device to function as though it were correctly soldered.

(c) Difficulty in accessing leads.
The troubleshooter may find it hard to get the troubleshooting probe on the device leads, in some cases, because they have none. In other, because the ends of the leads curve under the chip. And in others, because the devices are packed so closely together that there is no space between devices for test probes or pins.

(d) Solder bridges.
Because surface-mount devices are packed so closely together (sometimes with only 0,25 mm between traces), there is increased danger of forming unintentional solder bridges.

Solutions are available for each of these problems, and they all involve either the use of automated test and troubleshooting procedures or designing for testability.

4.2 AUTOMATED TESTING SOLUTIONS:

The key to the device identify problem is clearly automated testing. Automated test systems have access to databases that identify each part and its location on the board, making it unnecessary to label either the part itself or the board.

4.3 DESIGN SOLUTIONS:

The remaining problems are solved by designing for testability. Both the unsoldered joints problem and the difficulty in accessing device leads can be resolved by adding test "footprints" for each device, which are then probed instead of the device.

This approach eliminates both the possibility of getting a "good" reading when pressing on an unsoldered joint and the need to access the leads on the device in order to test them. The solution to the problem of unintentional solder bridges is to design multilayer boards, with the signal layers "sandwiched" in the middle and the components soldered onto the outer power and ground layers. With this approach, there is no solder on the signal layers, and therefore no chance of unintentional bridges. To allow access to test nodes from below (eg. by a standard bed-of-nails test fixture), one then drill holes ('via) through the layers. Each via must be located close to its corresponding device to avoid the possibility of probing the wrong device.

4.4 EQUIPMENT CONFIGURATION FOR AUTOMATED TESTING / TROUBLESHOOTING:

To test the surface-mount boards, Fluke set up two types of test stations. One for performing functional tests and one for troubleshooting. At the heart of both is the Fluke 9100 Series Digital Tester and Troubleshooter. The same system whose boards were being tested.

4.5 9100 SERIES DIGITAL TESTER AND TROUBLESHOOTER:

To understand how Fluke were able to fully automate the test and troubleshooting process for the 9100 Series boards, it is important to understand a little about the 9100 Series itself, since they used it both to develop the automated routines and to execute them. The 9100 Series offers automated digital testing and troubleshooting for all types of devices (surface-mount as well as through-hole), on microprocessor and nonmicroprocessor-controlled boards. Its built-in decision tree for guided fault-isolation lets it make intelligent decisions on which node-to-probe next, based on the reading from the previous node. One reason why the 9100 Series is so versatile is that it offers three ways to access board components, either via,

(a) microprocessor interface pods, or
(b) I/O modules, or
(c) a troubleshooting probe.

To functionally test circuitry on the microprocessor bus, one selects the appropriate microprocessor interface pod. The pod takes control of the bus and all bus-related devices, in effect replacing the board's microprocessor. To isolate faults with node-oriented troubleshooting, one can use either an I/O module or the troubleshooting probe.

The I/O module tests all pins on a chip at once, up to 40 pins at a time. (Since one can use as many as four I/O modules at once, one can in fact test up to 160 pins simultaneously.) The troubleshooting probe, in contrast, tests just one point at a time. It is useful for probing parts of the board that cannot be accessed with the I/O module, and also for testing higher frequency signals, up to 40 MHz.

The 9100 series is available in two models. The full 9100A digital test system and the 9105A digital test station. The 9100A comes with 2 M-bytes of RAM, a 20 M-byte hard disc, and two RS232C serial ports, and can be used both to develop test programs and to execute them. An optional programming workstation adds a standard CRT and QWERTY-style keyboard. The lower cost 9105A is functionally identical to the 9100A except for the ability to develop test programs, and is typically used to execute programs developed on the 9100A. In this configuration, Fluke chose to use the full 9100A with the programming workstation at all locations, because the 25-line CRT will display more test and troubleshooting information to technicians than on the 9100A's three-line display.

4.5.1 Equipment in the subtest area:

The test and troubleshooting operation is set up so that functional testing is first performed in the subtest area. Boards that pass these tests go on to be combined into sub-assemblies (after which they are again functionally tested). Boards that fail go to the troubleshooting and repair workstation. Equipment in the subtest area consists of two 9100A's, each connected (via an RS232C port) to an Intermec 9511 barcode reader. The barcode reader allows the user to automate the identification of the board and operator, eliminating the need for manual data entry. The operator simply passes the barcode reader wand over the board and the operator's badge (both of which contain barcode ID's) at the start of each test. The data of the test results can then be accessed by either board or operator ID.

FLUKE'S AUTOMATED TEST AND TROUBLESHOOTING SYSTEM

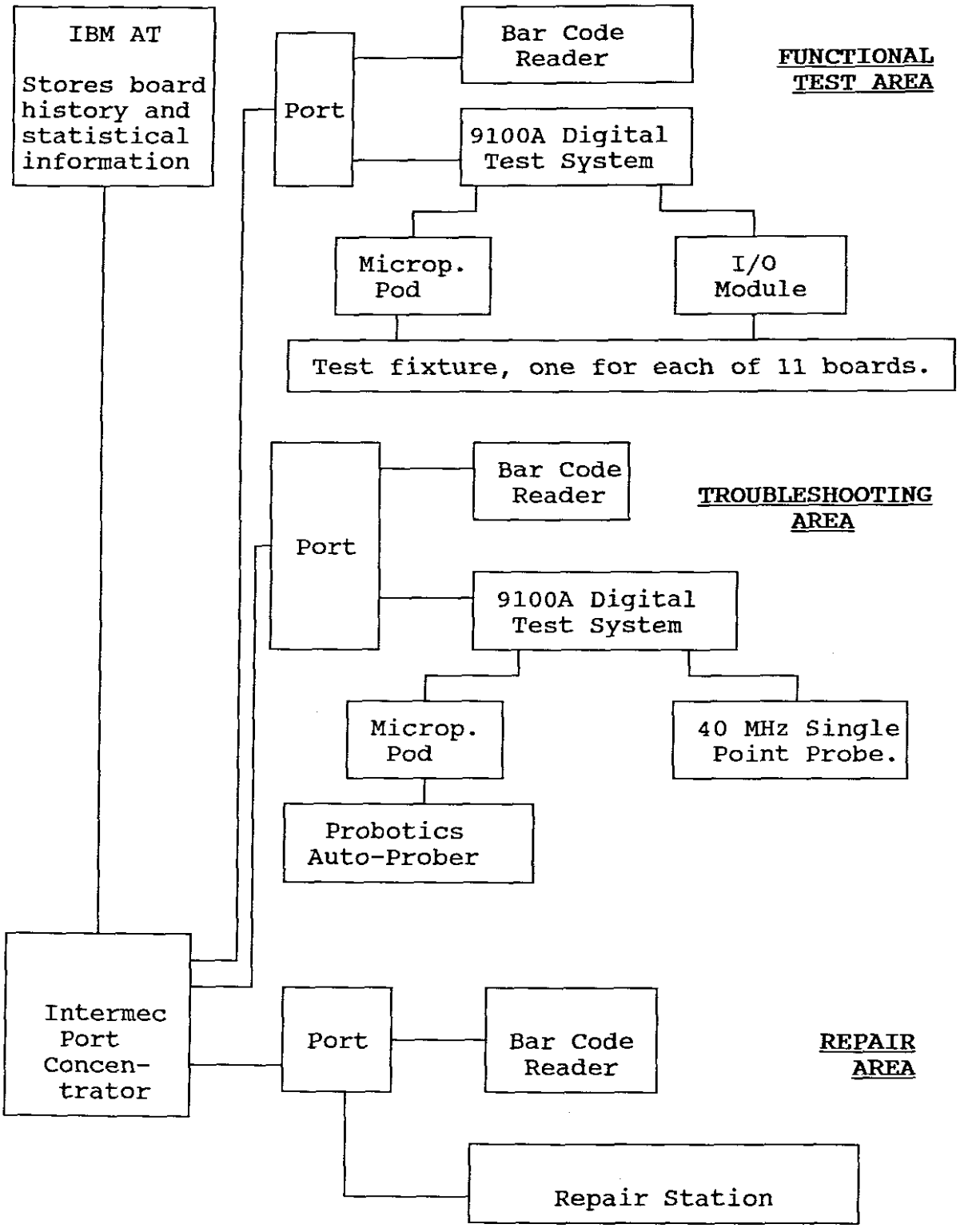


fig.4.5.1

4.5.2 Equipment in troubleshooting/repair area:

For each workstation in the troubleshooting/repair area, a 9100 is installed to control the troubleshooting sequence. Each 9100 is connected to both a barcode reader and a Probotics PCT-1 robot-prober through its two RS232c ports. The prober works much like a plotter, except that it uses the 9100's troubleshooting probe instead of a pen. It selects nodes and probes it then in response to information sent by the 9100. In addition, a Intermec 9161A port concentrator is added for both the functional test and troubleshooting/repair areas, to network all stations together. The port concentrator, which can poll up to 16 individual stations, is also connected to the library computer (an IBM AT with a 30M-byte hard disc). The AT acts as a file server for all test and troubleshooting data.

4.5.3 Developing the test routines:

Having set up the required equipment in each area, the next step was to develop the automated test routines that would allow testing and troubleshooting to be performed with minimal operator intervention. This step had two parts. Creating the functional tests for the subtest area, and developing the guided fault isolation routines for troubleshooting. Fluke created one functional test for the entire board, with a separate subroutine for each portion of the circuitry. They start by using the 9100's preprogrammed RAM, ROM, and BUS tests and added a variety of I/O tests, including tests for the floppy disc controller, RS232C ports, and exterior buses to other boards. When developing the functional tests, they also included troubleshooting `hints` that the 9100's built-in guided fault isolation decision tree could use in deciding where to begin probing a board that failed the test. That is, if the TE knew from experience that a board that failed the RAM functional test often had a problem with a particular pin, he would include a comment line in the routine recommending that troubleshooting begin with that pin. Developing the guided fault isolation (GFI) routines came next. This step is an essential part of automated troubleshooting, since these routines supply the 'intelligence` that tells the robot-prober where to probe. The 9100's built-in GFI decision tree makes this progress much quicker and easier than it would be otherwise. The decision tree uses a special back-tracing algorithm that combines basic troubleshooting rules with the board specific information provided by the test engineer in developing the GFI routines. Because this GFI algorithm has already been developed, the test engineer can enter the board-specific information in simple database format, saving a considerable amount of programming time. This information consists of six types of data files.

Stimulus routines, a reference list, a parts library, interconnectivity data, device location information, and know-good responses. But even these files do not all need to be created manually. The parts library is largely built into the system, and they were able to download the reference list, interconnectivity data, and device location information directly from the CAD files, so that only the stimulus and know-good response files had to be created from scratch.

4.5.4 Stimulus routines:

One of the first task was to write stimulus routines to exercise all nodes in all possible ways. For example, a data line to a RAM chip had to be exercised both for reading data out of RAM and writing data to RAM. Each routine had to be repeated for verification, as many as 100 to 200 times. All routines should involved several different forms of measurement (signature analysis, event counting, frequency counting, and logic levels). For this test it would be the best solution to start with the signature test first because it usually provides the most reliable data, and only when the signature proved to be unstable then it would be logical to move on to another form of measurement.

4.5.5 Troubleshooting/repair area:

To initiate troubleshooting, the operator simply positions the board on the robot-prober and selects the appropriate routine from a menu on the 9100. The 9100 takes over from this point on, freeing the operator to go on to another task, such as repairing a board that has already been through the troubleshooting process.

The 9100 begins the troubleshooting process by downloading the device location file to the robot-prober. It then sends its first command telling the robot-prober where to start probing based on the troubleshooting hints provided by the failed functional test. If the functional test includes more than one hint, the 9100 takes them in the order received. The robot-prober probes the specified node and sends the pass/fail results back to the 9100. The 9100 uses these results to decide which node the robot-prober should probe next. For example if the first signature is bad, the 9100 begins back tracing from that point. If the bad signature was found on an output pin, the 9100 directs the robot-prober to probe the previous output pin. If the first point probed turns out to have a good signature, the 9100 goes on to the next troubleshooting hint in the functional test results.

If the data in the known good response file suggests that a bad signature at a particular node may be due to a problem several nodes earlier, the 9100 will try that node first rather than single step back tracing. The total troubleshooting process takes anywhere from a few seconds to a few minutes, depending on the complexity of the board and where the fault is located. When the fault has been isolated, the 9100 signals the operator that troubleshooting has been completed. However, the operator is free to complete the task at hand or come to a logical stopping point before responding. When troubleshooting and repair are completed, the board goes back to subtest for a repeat of the functional test sequence.

4.6 THE BENEFITS OF AUTOMATION:

By automation the test and troubleshooting operation ,it will definitely enhance the productivity and throughput. Also it will provide the user with several other benefits as well. Overall he will see improvements in three categories:

(a) the troubleshooting results themselves,
(b) operator productivity,
(c) and management of the entire operation.

4.6.1 Better troubleshooting results:

Fluke found that using the robot-prober to perform node oriented troubleshooting not only improved their throughput, but also gave them more accurate and reliable results. This is due to the robot-prober"s ability to:

* always probe in the correct place,
* always apply the same amount of probe pressure,
* and touch the test 'footprints' only, rather than the device itself.

As a result, there is no danger of accidentally contaminating the device with oil from the fingers, or accidentally discharging static electricity.

* Eliminate the factor of operator fatigue. Operator fatigue can be a problem with any tedious, repetitive task, but it is especially significant in the case of surface-mount boards because of the extremely small size of the devices and test points and also the fact that they are packed together with such density.

4.6.2 Enhanced operator productivity:

Fluke also found that automating the test and troubleshooting functions significantly enhanced operator productivity, not only because the operator could perform other tasks while the robot-prober was doing troubleshooting, but also because networking individual workstations together made all of the relevant data instantly available at each workstation. The operator has no need to stop and look up the correct test or troubleshooting procedure for a particular board. Instead, the operator just selects the board type from a menu and the 9100 loads the proper test or troubleshooting sequence. The operator has no need to spend time determining what a board is doing in a particular area (eg. which tests it has failed, or which component needs to be replaced). In manual test and troubleshooting operations, masking tape is usually used to identify a board's problem. Masking tape sometimes comes off, and handwriting may be illegible or it is possible to do further damage to the board when applying or removing the tape. With automated testing and troubleshooting, in contrast, all the necessary information is available on the 9100 just by passing the barcode wand over the board.

4.6.3 Better management:

The data collected by the 9100 also has another benefit. It offers management the opportunity to gain a better understanding of how smoothly the test and troubleshooting operation is functioning. By analyzing this data, management can identify possible problem areas and take action to resolve them before they become serious. Specifically, this data can be used to achieve the following improvements. Test and troubleshooting data can provide important feedback for process control. For example, management can check to see if certain types of defects are showing up regularly, and if they are, take action to correct them. Similarly, it will be immediately evident if particular board is having repeated problems, in which case it may be more cost-effective to throw it out rather then keep trying to fix it.

Data gathered by the automated test and troubleshooting system can also be used to provide feedback to design engineers. For example, if a particular portion of a board's circuitry is having repeated problems, the design engineer may want to change the design, or possible specify different components. If certain test or troubleshooting routines have repeated problems, this information can be send back to the test engineers so they can rewrite the sections in question.

The automated test and troubleshooting system also allows supervisors to gather data on operator productivity, so they can help operators become more productive. A final benefit of automatic testing is that it saves significantly on the work when developing test routines. Many of the routines used in production are in fact developed by designers during the design stage of a project to verify that the circuitry functions as expected. Rather then reinventing the wheel at later stages, these early routines can be stored on the 9100 where they will be available to all who may need them. When the product is ready for production, test engineers can then just modify and change the existing routines rather than starting over from scratch.

Each of these benefits has a positive effect on the company's bottom line, because each one reduces the cost of doing business. The ultimate benefit of an automated test and troubleshooting system then is, that it makes a company more competitive and increases profits.

5.0 LATEST TECHNOLOGY OF TESTING

5.1 INFRARED TESTING OF ASSEMBLED PRINTED CIRCUIT BOARDS:

Researchers of the CSIR's Division of Production Technology have recently developed a diagnostic station for the semi-automatic testing of populated printed circuit boards (PCBs). Employing infrared thermography and image-processing techniques, the equipment was constructed at the Division of Production Technology's laboratories. It is equipped with a comprehensive suite of custom software.

South Africa's electronic manufacturing industry does not yet approach a 'zero defect' rate in PCB assembly, and thus the functional testing of such devices forms a significant activity in the manufacturing process. This is especially true in cases where a variety of complex products are assembled in small quantities.

Full-functional testers and other ATE systems perform this test effectively, where large production quantities justify the capital expenditure and running costs involved. Considerable time and effort is needed for these systems to be set up for a new PCB type.

A low cost diagnostic testing facility for PCBs, requiring very little in the way of setting-up and programming, would provide an interesting alternative for small production runs, reliability studies on prototype designs, and maintenance applications.

Infrared thermography, the study of thermal patterns emitted in the medium and high infrared bands by all bodies above absolute zero temperature, is a most useful tool for detecting a variety of faults on an operating PCB. This technique has been used informally in the electronics industry, as evidenced by various articles and publications. These infrared devices have ranged from simple handheld spot sensors for locating 'hot-spots' to fully fledged thermal imaging systems.

Researchers at the Division of Production Technology conceived the idea of an integrated workstation for the thermographic testing of PCB's, consisting of a low-cost scanning unit, combined with extensive microcomputer hardware and powerful display/analyse software specially designed to evaluate the comparative performance of the PCB under test. The system would be capable of detecting a wide range of PCB faults. Low cost setting-up of overheads, an affordable cost structure, ease of operation requiring no special skills were considered to be paramount importance.

5.2 THREE STEP PROCESS:

The design concept formulated as the most appropriate for the realisation of these distinct phases. These correspond to the functions of thermogram display, and analysis by comparison with a reference signature. Acquisition of the thermal image is achieved by sequential scanning of the PCB under test, using a relatively low-cost spot sensor, and moving the PCB beneath the sensor. This was implemented using a custom-built X-Y positioning stage and motion control unit, as well as a Mikron Infraducer uncooled detector in conjunction with a 12-bit data acquisition module. An intelligent controller, reporting to a supervisory computer, supervises the motion control. The PCB under test is placed on the table in a simple fixture which merely restrains the board mechanically and supplies appropriate power, as well as any critical stimulus signals (many PCB's are successfully tested with only power supplied). The X-Y table is stepped under software control and the thermal emission of the various components continuously sampled via a 12-bit A/D, so as to build a thermal image of the PCB under test in the computer memory. This strategy certainly achieves the objective of low cost. It is of an order of magnitude less expensive than an equivalent thermal imaging front-end. Apart from cost, other advantages include repeatability in the spatial domain. This is inherent in the structure of the image acquisition system, namely a rectilinear arrangement of rigid construction, which effectively eliminates parallax and tilt effects, and generally eases the problem of registering successive images. A multiple-output, programmable power supply is incorporated in the workstation so that appropriate voltages can automatically be applied to the board under test according to a pre-stored 'recipe, prior to initiating the scan. An upgrading MS-DOS computer with a hard-disc acts as operator interface, graphics display unit, storage device, hardware supervisor and data acquisition unit, in addition to running the display and analysis programs.

5.3 SOFTWARE:

Software was developed in a Turbo-Pascal environment, and currently comprises some 12000 lines of source code. The operator interface is entirely menu-driven, with extensive use being made of windowing techniques and most operator interaction taking place via a 'mouse'. Features provided include PCB identification and a PCB recipe library stored on hard disc. Other features include display options, normal thermal limits and the like.

In spite of the comprehensive nature of the software, it is extremely convenient to use, the default options 'talking' the first-time through the entire procedure of PCB testing. At the same time, sophisticated manipulation techniques and evaluation aids are available in the background for the skilled user. During a scan, the thermogram is complied in the system's memory and converted to display format.

The image data are normalised for ambient temperature, in order to compensate for fluctuations in the latter, thus permitting the comparison of thermal images acquired under differing ambient conditions. An advanced graphics facility permits the display of a 16-level pseudo-colour thermogram, utilising various dynamic thresholding techniques, to be built up on the screen in realtime during the scan.

The thermal scale of the display can be altered, and a cursor allows a readout of the apparent temperature of any point on the image, its position, size, orientation and superimposition on other images. These display features are intended as evaluation aids and operate independently of the analysis program. A typical use of these would be in the investigation of the thermal management of prototype PCB designs as part of a reliability study. Analysis of the PCB performance is accomplished by automatic comparison with a reference model, compiled from one or more similar PCBs of known acceptable performance. This model consists of a thermal signature, power supply voltages, pins, typical operating currents and optional component placement details. A result image is produced, using proportional different algorithms, and is displayed together with the result of a numerical correlation check.

A go/no-go display which highlights thermal anomalies exceeding the limits of normal component tolerances is also generated from the difference data. Selected results may be summarised on a graphics printer incorporated in the system. These analysis routines operate directly on the 12-bit image data, and can all be achieved in realtime, causing no perceptible degradation in system operation. To summarise then, a totally new PCB can be tested by fixing it in a simple jig which also supplies power, and by choosing a set of scan parameters. The initial scan is stored as a reference, after which PCBs of a similar type can be tested at will. This preparation need literally take no more than a few minutes.

5.4 TEST RESULTS:

The results of tests on a variety of PCB's demonstrate clearly the ability of the system to detect a wide spectrum of faults, with a minimum of operator intervention and with virtually no preprogramming or setting-up overheads. Detectable faults include:

* missing components,
* reversed components,
* components with wrong values,
* faulty components,
* short-circuited or open-circuited components or unsoldered leads,
* short-circuited or open-circuited PCB tracks or through plated elements.

Results show the techniques to be tolerant of variations due to legitimate component tolerances, this being adjustable via the go/no-go limits. Naturally there will be cases where certain of the above fault conditions will not result in thermal anomalies and will therefore not be detectable with this technique.

One example is where no current is drawn through a component (eg. its circuit is completed through some off-board element). The presence of such a component may still be detected by virtue of its emissivity characteristic, but a wrong value or unsoldered component would remain undetected in this case.

5.5 APPLICATIONS:

The technique has potential for application as a diagnostic tester in its own right, especially in the smaller electronics concern, where it could fulfil the multiple roles of reliability analyser for prototype designs, semi-automatic tester for production runs, and maintenance diagnostic tool. In the larger electronics manufacturing environment, the infrared diagnostic system would also provide a useful pre-screening facility for off loading the full-blown, full-functional test (FFT) installation. There is a growing realisation in the industry of the need to reduce unnecessary loading off FFT installations.

6.0 IN-CIRCUIT ECONOMICS

6.1 REPAIR RATIO:

The features on an in circuit tester with advanced, high performance capabilities were discussed up to this point. The fact is that if the user can catch more faults earlier in the test/repair process, then he will derive very significant economic benefits. The main question for any repair or test centre is to find the point on the curve, where the quantity of the different types of faults a tester can catch, cross with the funds required to catch those faults. A simple algebraic method can be used to get to some sort of assumptions.

* The cost of testing and repair increases by a factor of ten through each successive level of testing.
* A conventional in circuit tester covers the catastrophic faults which are nominally around 90% of all PC card problems.
* The balance, that is 10%, must be covered at the next level of testing.

This is called the 90/10 ratio. The ratio is normally dependent on the type of equipment to be repaired.

Example:
Let x represent the cost per fault at the in circuit level.

Level	Test type	Cost/fault	Ratio	Cost	% of total cost
1	In-circuit	x	90 %	90x	90/190 = 47%
2	Functional	10x	10 %	100x	100/190 = 53%

The overall cost is 190 cost units. The conventional in circuit tester shares only 47% of the cost of test and repair, where 53% is at the functional testing level.

Lets take another example:

Ratio 95/5.

Level	Test type	Cost/fault	Ratio	Cost	% of total cost
1	In-circuit	x	95%	95x	95/145 = 66%
2	Functional	10x	5%	50x	50/145 = 34%

The overall cost is now 145 cost units. The conventional in circuit tester now shares 66% of the cost of test and repair, where the functional tester incurs 34%. The overall cost has dropped by 45 cost units, which represents a net decrease in overall cost of 24%. So by getting 5% more catastrophic faults, which means 5% less faults on the more expensive level, the user will have a overall cost saving of 24%.

Since 24% divided by 5% is approximately 5%, then with respect to the base line 90/10 ratio, which means for every additional percentage point covered by the high performance in circuit tester, it will give 5 percentage points of overall cost savings.

6.2 TURNING DATA INTO INFORMATION:

What's the real difference between data and information? The difference is in their respective application. For example: when a board fails, it's either because of some integral part of the board or some component which is mounted on the board. In either case, there exists data associated with this failure.

* Data which is related to the PCB being tested.
  - The PC board serial number.
  - The component(s) or trace(s) which failed, etc.
  - Even the specific type of test which was in progress.
* Data which is related to the manufacturing process.
  - What tester was performing the test?.
  - What was the time and date of testing?.
* Data which is related to the testing process.
  - How long did the test run?.
  - Who was operating the tester?.

6.3 CONTROLLING THE UNCONTROLLABLE:

The goal is to create a well-controlled process. That's the bottom line in productivity, and there can be no substitute. The manufacturing, testing process will want to make real time decisions based on real time information. Once again, timing is most important. If the decisions are untimely, they are useless. So, to control the manufacturing, testing process, the TE must be able to access and interpret useful data in real time? But there exists a human element and that's the decision making process where the information is the intelligent presentation (tabulation) of the raw data. The key word here is "networking". A networking system is a centralized computer facility which ties the ATE together to pool all the ATE test/repair data.

A state-of-the-art networking system should provide capabilities to:

* Communicate with all factory ATEs.
* Perform fast and accurately with user-friendly software for the purpose of system interaction and report generation.
* Be flexible -- able to accommodate both the present and future needs.

The bottom line here is that the networking should be able to help the user make intelligent, real time decisions which are based on everyday manufacturing ailments.

Understanding both a manufacturers process and his requirements is a mandatory prerequisite for understanding what type of ATE equipment to specify. FACTRON offers a full breath of testing, repairing and networking equipment and are probably rated number one for in circuit and functional testers in the world.

Keeping in mind that the prospective user are not just looking for a tester, his looking for a test solution... a total test solution.

The sole agents should provide the following customer supports:

* Training.
* Maintenance.
* Parts.
* User meetings.
* Field expertise.
* Customer services.
* Contract programming.
* Documentation.
* Fixturing.

6.4 CUT SPARE BOARD INVENTORY BY 30% WITH DISTRIBUTED REPAIR:

A properly planned, distribution repair operation can significantly enhance a company's profitability and improve customer satisfaction. Implementing such a program requires a thorough knowledge of the customer base, what repair volumes are likely to be, and what sort of fault spectrum can be expected. Armed with this information, the Field Service Manager can determine the best way to structure a repair facility.

6.4.1 Field Service - a background:

It may sound harsh to term field service the unwanted stepchild of electronics manufacturers, but it is, essentially, a flawed product. That is exactly what field service is about-resolving errors created by manufacturing and the shortcomings of poor design. Although unfortunate, it is impossible to avoid it in the world of high technology. Manufacturers must consider the possibility of design flaws. If a problem occurs in the field, who is going to investigate and report back to the factory and who is going back out to the field to implement the necessary design changes?

These problems have faced electronics manufacturers for decades. Until recently, a computer's size precluded a technician from carrying the product normally as could a TV repair technician. Also, the number of installed computers was far fewer than to use the same example - TV sets. Computer manufacturers could not economically justify a large group of sales/service centers. Thus was the field service group born. This small army of personnel had the sole responsibility of installing new computer systems and diagnosing problems when they arose. Such geographically strategic groups cost money, but the price of a customer system was relatively much higher.

Field service technicians have historically performed repairs by replacing the failing PCB, since the technical requirements of repairing boards were prohibitive in terms of training and equipment, and the customer demanded that the system be operational as soon as possible. The best compromise was to swop boards. This solution however, created a new problem. What happens to the bad PCB's? The central repair depot was thus born.

CENTRALIZED REPAIR PHILOSOPHY

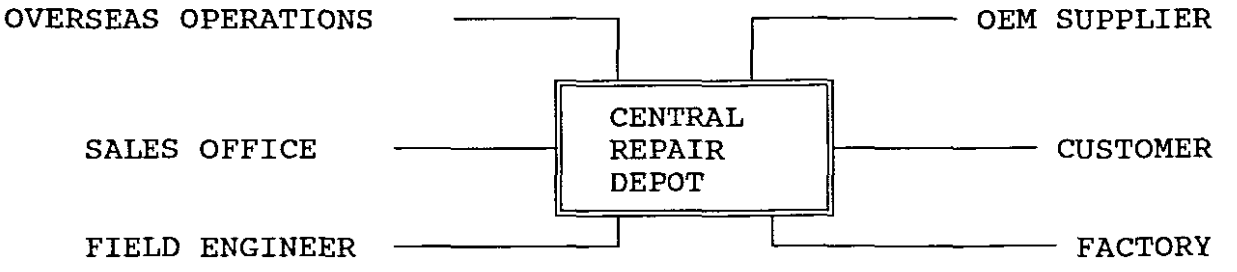


fig.6.4.1

6.4.2 Centralized repair philosophy:

Manufacturing personnel realized that if they performed repairs they would be dealing with different PCB problems than those that they were accustomed to, such as multiple revision levels, obsolete designs and dirty PCB's. Repair depots needed to be large scale industrial versions of the local garage, big enough to serve a large number of customers, but flexible enough to handle the problems faced in service. The central repair facility was usually located in or near the manufacturer's main facility. It served not only the field service group, but also the customers directly, the overseas sales service facilities and, in some cases,the manufacturing group itself. In the case of OEM parts, the depot would ship defective assemblies, and redistribute them when they were returned. Depending on the size of the parent company, the depots could be as large as a normal manufacturing facility, complete with accounting, shipping and scheduling departments. All of that plant, personnel and equipment was profitless overheads.

6.4.3 The march of progress:

In the 1980s, technology offered a new child, the personal computer (PC). The price and packaging of the PC created a revolution that made PCs almost as numerous as TV sets. However, a new service problem development. The cost of service, became a too large percentage of the retail price of the system. Ten years ago a mainframe computer cost approximately R3 000 000. If 5% of the cost was reserved for warranty repair, that would mean R150 000 was allocated for service. A PC of equal power today sells for R36 000. 5% of this cost is R1800. With this limited amount of money, either the volume of systems sold had to be phenomenal, or a new service philosophy was needed. Added to this was the element of competition that began driving down the price of personal computers to unbelievably low levels. Today, some PCs can be bought for less than R3000 and the 5% allocation for service is R150.

6.4.4 The force of change:

Three forces are driving this change in service, viz cost, profitability and time. The second has already been discussed. The next is a new problem for service. Cut-throat competition in the industry is forcing companies to look for new sources of revenue. Service is one such source that for years has been waiting to be discovered. If customers want quality support after the warranty ends, why not make them pay for it?

The desire to tap this new source of revenue spawned concepts such as service contracts with levels of call-out speed. These are grand ideas, but they must be implemented correctly to be profitable. The last driving force, time, is an old one, but it must be considered in new ways. The customer's main concern has always been to make the computer operational as quickly as possible, which is one of the reasons that the board swop philosophy was originally adopted. Time has become a critical factor in the repair of a defective PCB, because the longer the PCB is in the repair pipeline, the longer the assembly is out of use for customer support. Because customer satisfaction is one of the primary goals of a service organization, extra PCBs must be available while the defective inventory is lost in the pipeline. However, with extra inventory and shipping costs, how can a service group remain profitable?

6.4.5 The board repair pipeline:

By examining a typical repair pipeline, it can be seen why it is such a problem.

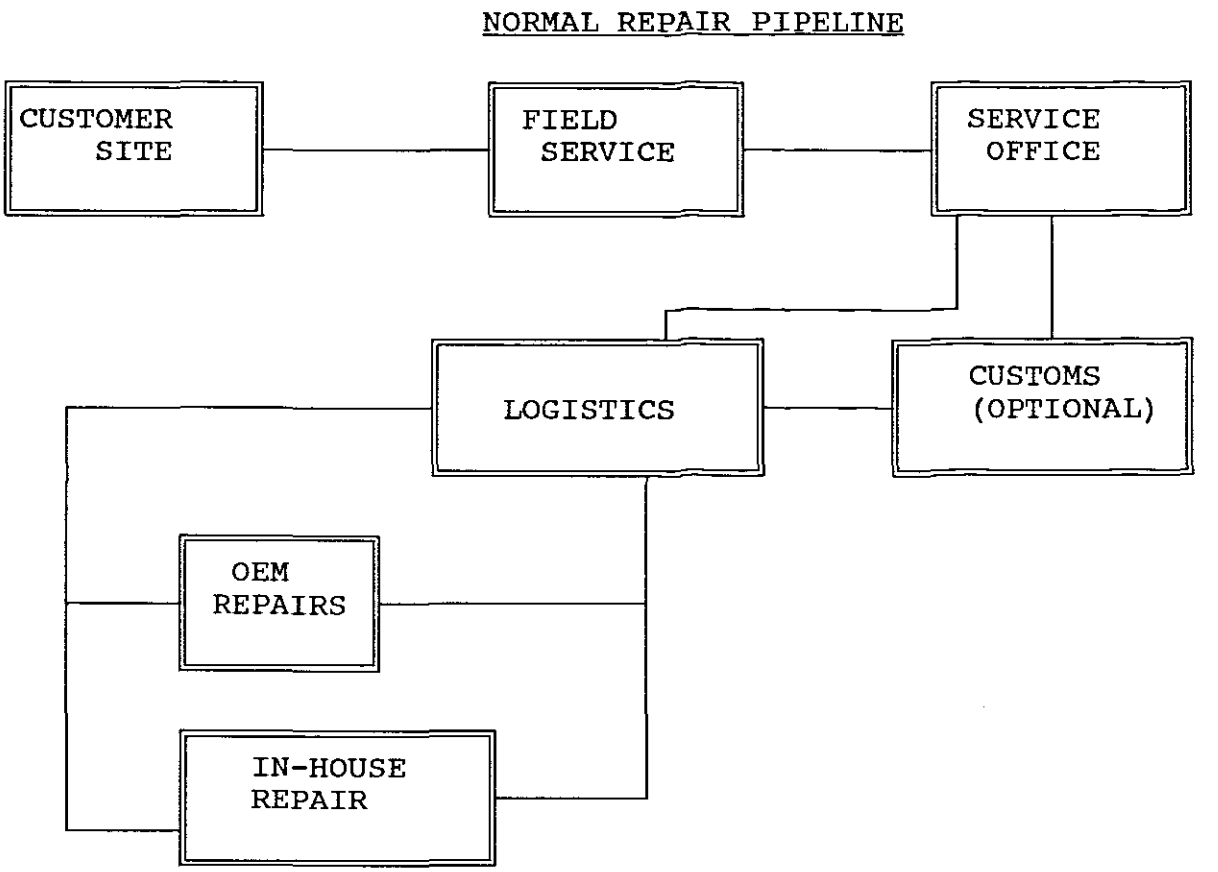


fig.6.4.5.1

A customer reports a down system to the service centre. The trouble is diagnosed over the telephone, and a PCB replacement is sent to the customer by overnight courier. The next morning, the customer replaces the defective PCB with the new one, and later that week a field engineer picks up the defective PCB. Because of other service calls and interruptions, the service technician does not send the defective PCB back to the regional office for several weeks. Once the PCB is at the regional office, it may be held until enough defective PCBs are available for shipment. They are then shipped to the repair depot by the most economical means. When they arrive at the depot, the PCBs must be sorted into types and, in some cases, into vendors. OEM products are often shipped back to the manufacturer, and the remaining PCBs are scheduled into the repair cycle. Once repaired, they are sent back to the regional office. The process from shipping to receiving can take anywhere from several weeks to several months. The entire process from customer to repair and back into the field can take anywhere from several months to a year. During this time, while the PCB is in the pipeline, the service organizations must have back-up spares.

By shortening the pipeline, the time to return the PCB to service would improve, and service could thus rely on a lower spares inventory, which reduces costs and increases profitability.

BOARD 'FLOAT' REPAIR PIPELINE

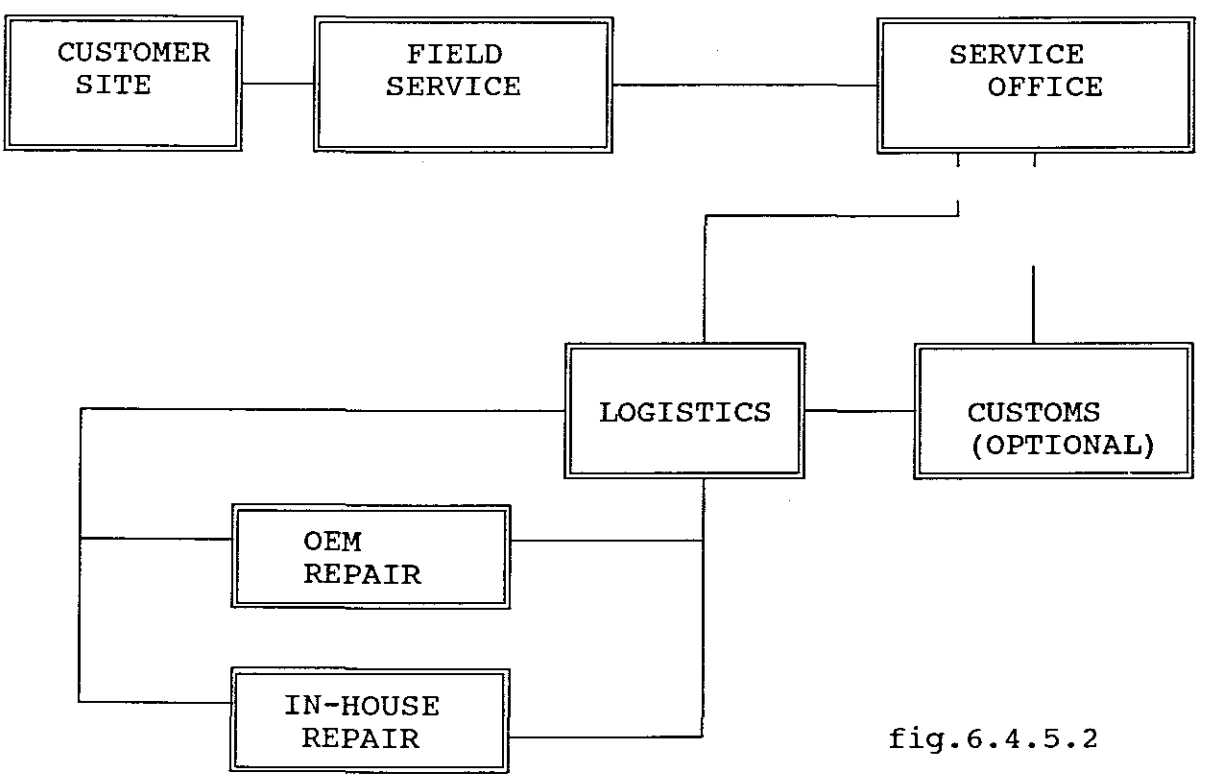


fig.6.4.5.2

But how can the pipeline be shorted? Service companies cannot control the customer, the freight companies or the repair depot. But what if they could avoid sending the bad PCBs back in the first place? The service time could be reduced by a large margin.

6.4.6 Distributed repair:

In the customer service industry, the central repair depot has been bypassed for years. These companies have been accustomed to operating on low margins and have developed a cost-effective strategy for repair. For example, TV and radio companies solicited the use of local service organizations, which performs most of the necessary repairs. Assemblies that were too difficult to repair locally were sent back to the main repair depot.

The strategy is known as the distributed repair philosophy.

DISTRIBUTED REPAIR PHILOSOPHY

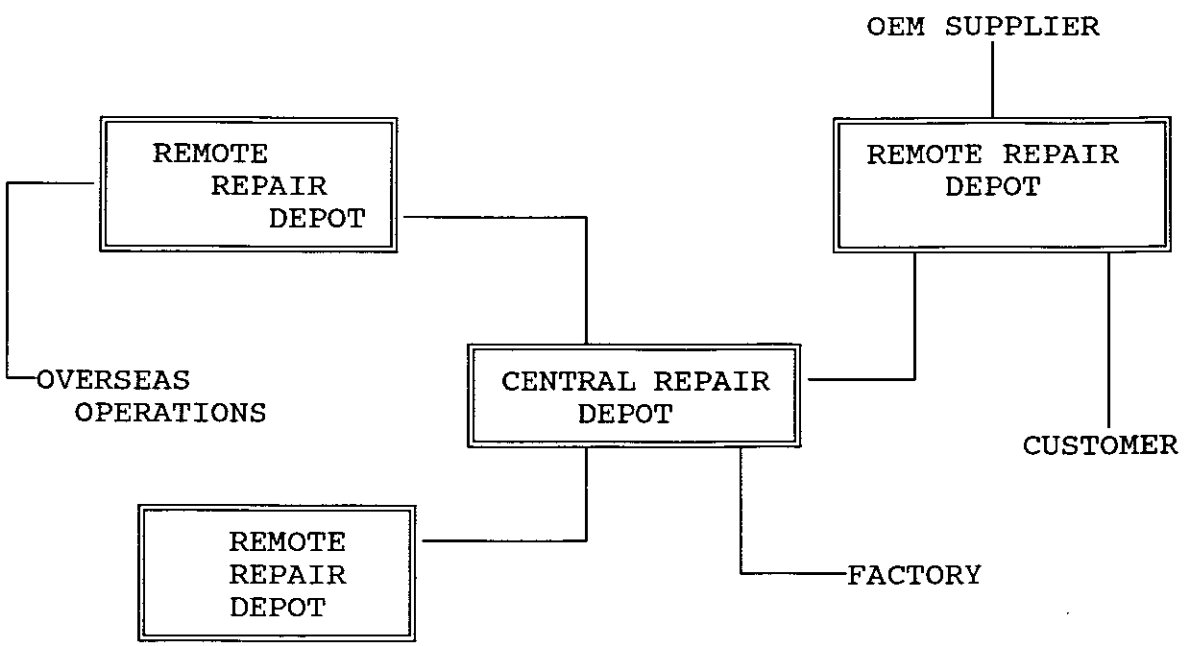


fig.6.4.6

As many repairs as possible are performed in the field, which cuts shipping costs and repair time in large organizations. Because this strategy worked in the consumer service industry, it would be expected to work in the computer service industry. However, it is not as simple as it sounds.

6.4.7 Location considerations:

To complement the distribution repair philosophy, location should be the first consideration. By studying the field returns and the locations from where the defective assemblies come, one can determine the correct locations for repair depots. Depots should be located near major transportation centers, which will help to accelerate the delivery of PCBs to and from field technicians and will also help control shipping costs.

6.4.8 Expected work volumes:

The repair centre's size needs to be determined by considerations such as PCB volume. The figures in this Table were compiled in a survey by the Association of Field Service Managers in the USA, and offer some average percentages and ratios for a typical repair depot. Although these figures may be higher than those of other depots in operation, the percentages and ratios still apply in a smaller application.

AVERAGE PERCENTAGE AND RATIOS OF PCB's SENT TO A TYPICAL REPAIR DEPOT:

	Digital	Analog	Hybrid
PCB's Annually	11850	3320	2830
Batch Size	122	56	82
Different PCB's	163	65	122
50% of PCB Volume	32	14	49
Tested Good	3555	1129	821
Average Turnaround	4 weeks	4 weeks	5 weeks

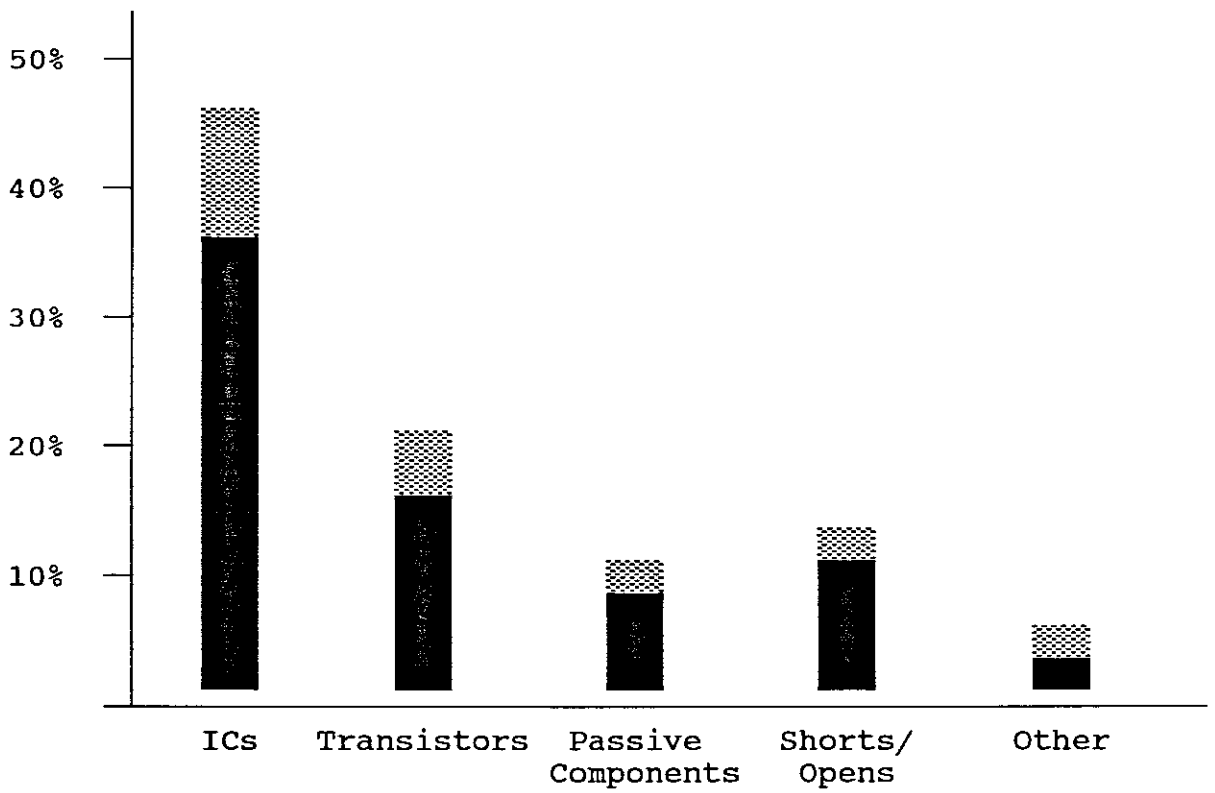
The annual volume of PCBs in the depot depicted in this Table is on a scale with a medium sized manufacturing operation. However, the batch of PCBs to be repaired at a given time, as well as the number of different types of PCBs, stems from the fact that service is responsible for everything the company has ever manufactured. The low batch rates relate to the nature of service and infant mortality.

Regardless of PCB type, a repair depot must be designed to be responsive to change. It should be ready to repair any PCB that comes along. Another big problem is the number of PCBs that pass test. Surveys indicate that more than one third of all PCBs going into the pipeline will pass. For such reasons, when planning a depot, a good go/no-go test for as many PCBs as possible should be included in the test strategy.

6.4.9 Which faults to repair?:

After deciding where to locate the depot, and the approximate size of the facilities, one should determine what is to be repaired. The information in the Table provides a clue. The percentages for a range of potential faults is shown in the next figure. (note that the percentages do not necessarily add up to 100%.

SERVICE PCB FAILURE MODES



This figure indicates that the biggest problem is faulty IC's. Almost 50% of all PCB problems relate to these devices. Device failure mechanisms include infant mortality caused by insufficient burn-in time at the factory, but the most prevalent failure mechanism is static electricity, which destroys the input or output stages of the device.

In this application, a 'pin faults' test may be adequate to verify the failures. This type of test represents the minimum that is required to ensure that no input or output pin is stuck-at-one or stuck-at-zero. The next three problem categories, transistors, passive components and shorts/opens, constitute the balance of most problems. Note that shorts/opens are at the opposite end of the fault spectrum, compared with manufacturing. It is known that the PCBs worked at one time and should not be present. Normally, shorts found on a field return are customer-induced by poor repair practices. The 'other' problem category relates to physical damage, such as cracked PCBs or missing components.

6.5 ATE: A COST-EFFECTIVE SOLUTION:

More service facilities are turning to some form of automatic test equipment (ATE) to implement repair operations, especially in light of the trend towards smaller, more powerful, less expensive and more ergonomic ATE product offerings.

An important consideration when closing ATE is that functional choosing such as emulators which are good go/no-go testers, but are slow in diagnosing component faults. These functional emulation testers fit well if the plan is to weed out good PCBs rather than repair them in the field, but remember that emulators are a good investment only if the number of types of PCBs is low, because they require extensive program development time (an average of 4-6 man-weeks per test program).

In addition, the level of technical skill required to program an emulator is generally higher than that required to program today's generation of in circuit testers. In circuit testers, on the other hand, are excellent either in an environment with a high number of PCBs types, or for repairing PCBs to component level. In circuit testers can deal with large numbers of PCB types because they require relatively short test program development times, viz an average of one man-week per test program.

The main disadvantage of in circuit testers designed for service is that they use a test clip to access the device under test, which can limit throughput. Another point to consider is that the latest generation of in circuit testers, eg the 635 service tester from Schlumberger Technologies, offer greater fault coverage than earlier products, with improved test hierarchies to increase throughput. Perhaps a compromise strategy should be considered, which uses both testers, the emulator as the go/no-go test system and the in circuit tester as the diagnostic tool.

6.6 CONCLUSIONS:

What does all of this mean to the Field Service Manager and the service organizations? At a minimum, by adopting a distributed repair philosophy based on the latest ATE, the service organization will run more smoothly because the repair pipeline will be shortened, cutting space PCB inventory by 30% or more.

Initial justifications will naturally depend on how the factors described in this article interact with a specific product. But there is a very good possibility that distributed repair will save a service organization time and money, as well as improve customer satisfaction.

7.0 REFERENCES:

1.0 **Complete Guide to DIGITAL TEST EQUIPMENT**, by Walter H.Buchsbaum.

2.0 **The Primer of High-performance In-circuit Testing**, Factron - Schlumberger, 1985.

3.0 **Cut spare board inventory by 30% with distributed repair**, by Factron Schlumberger, from DATAWEEK, April 22, 1988.

4.0 **Automated testing of surface-mount boards**, by Jim Clodfelter and Mike Petterson, from DATAWEEK, July 1, 1988.

5.0 **OLIVETTI tecnost PST100 test system that uses the in-circuit test technique**, DATAWEEK, July 1, 1988.

6.0 **Infrared testing of assembled printed circuit boards**, DATAWEEK, July 15, 1988.

IDENTIFIER CARD TESTER

PART 2

1.0 INTRODUCTION:

1.1 PURPOSE OF THE IDENTIFIER CARD TESTER:

The ID tester was built as a repair aid for the technicians who must repair the "Identifier Program Control Sender Card" (ID card). See figure 1.1 (Identifier system in the auto-mechanical exchanges) and figure 1.2 (Program control and Impulse Sender card). There were no other test facilities available for these type of cards and it was very difficult and time consuming to find a fault on it. The technician must basically remove each component from the card and test it separately. A multimeter was the only type of test equipment you could use because there were no input signals available or a rack where you can get some sort of input signals from.

It normally takes a technician half a day to prove a card to be faulty or to get a fault. Most of the time he just tests the resistors, capacitors and transistors and if he didn't find a fault he had to send the card back to the region, "No Fault Found".

With this ID tester (see figure 1.3) a technician is now capable of handling up to ten cards a day, depending on the type of faults present. Instead of just using a multimeter he can now make use of a oscilloscope as well. He will be able now to compare the output signals of a faulty card to a reference card at the same time, because all the input signals are equal on each card.

The ID tester also makes provision for a rough adjustment. Most of the faulty cards are being tampered with in the exchange, and the first thing the technician in the Repair Centre must do is to re-adjust the card first so that the timing sequences pass on the ID tester. If the timing sequences pass he will then be able to see which output fails by just looking at the Display unit. When the two led's underneath each other go on\off at the same time it indicates that this output is functioning perfect. If the two led's do not flash together then the faulty output can be determined from the circuit diagram and one can immediately start tracing the fault with the aid of an oscilloscope.

Some of the outputs also have a third led (white colour) to indicate if the timing of the specific outputs are equal etc. This led will glow "RED" if the outputs between the Reference card and Unit Under Test card do not agree, and glow "Green" when the two outputs do compare.

This comparator method will allow the technician to adjust the faulty card to a point where he can start looking for the real fault, instead of wasting his time, trying to see what's going on. In a few occasions it will be necessary to do a finer adjustment in the exchange rack itself.

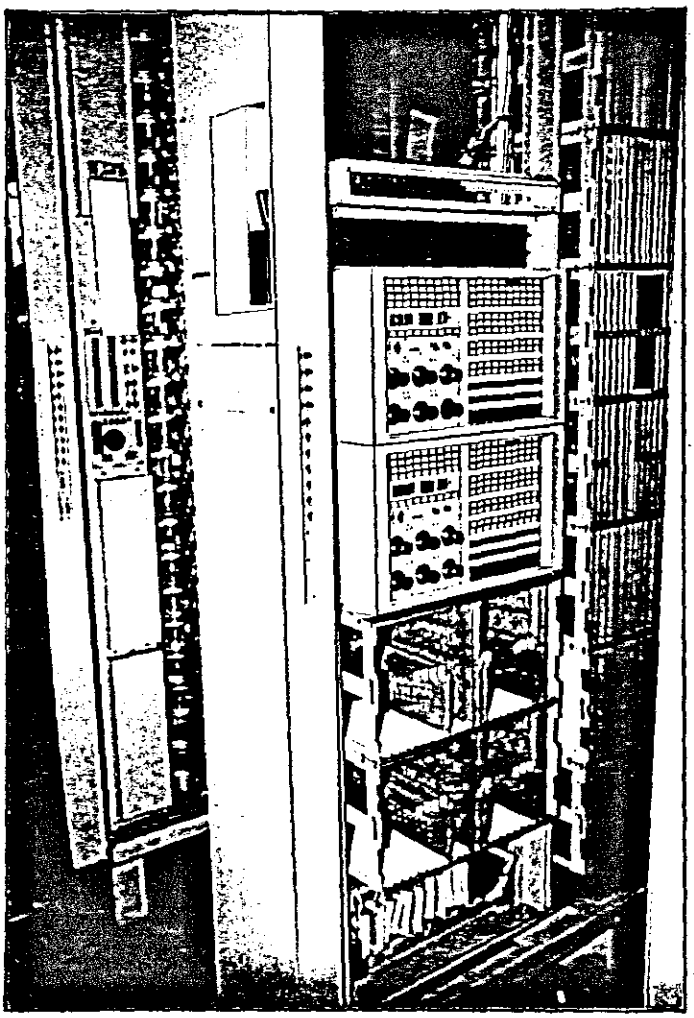


Fig 1.1 Identifier system in the auto-mechanical exchanges.

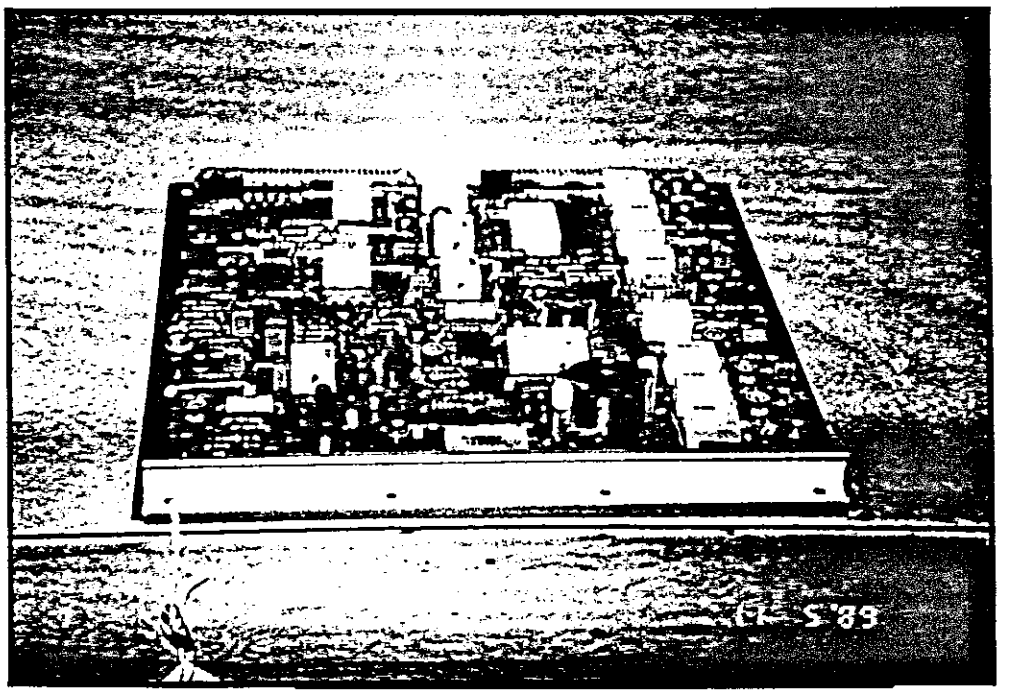


Fig 1.2 Program Control and Impulse Sender card.

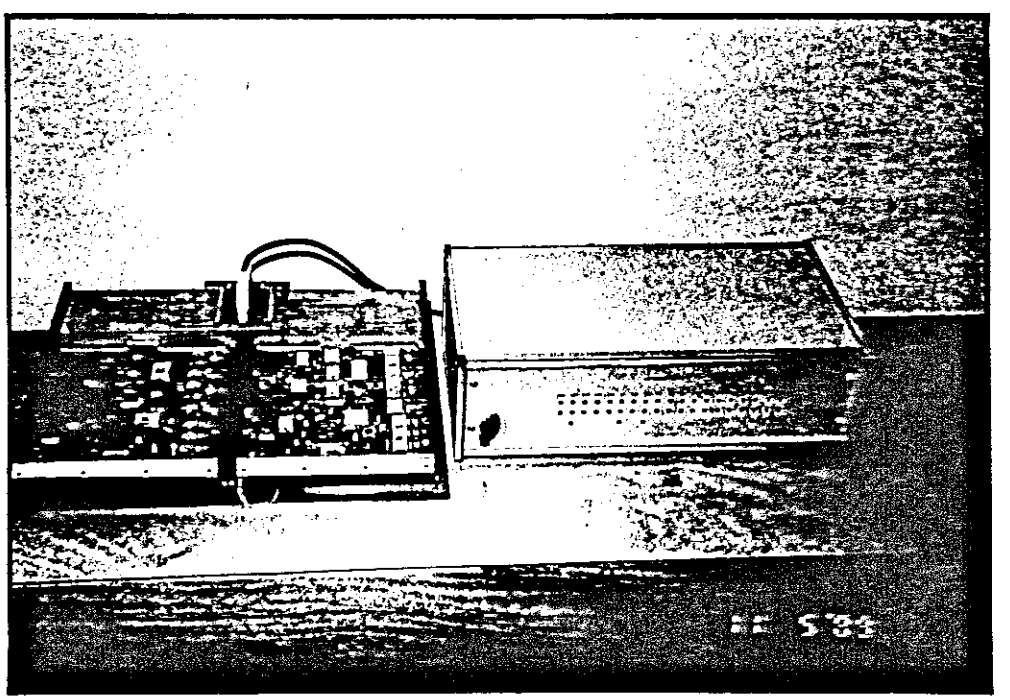


Fig 1.3 The "Identifier card tester" with outrigger.
(two "Identifier" cards plugged in)

1.2 GENERAL CIRCUIT DESCRIPTION OF IDENTIFIER CARD IN THE SYSTEM:

1.2.1 Pulse sender:

The pulse sender primarily consists of an MT-component (M10, T16) which switches the primary of the shell-type core transformer L1. (See drawing A30238-X742-X-*-7611 of the Post & Telecommunications department for the circuit diagram of the "Program Control and Impulse Sender card".) The secondary of the transformer represents the actual identification pulse generator. As the identification pulse is longer and stronger than the program control pulses, a 10 mm Φ ferrite core with a larger change in the magnetic flux is used for this MT-component.

The identification pulse starts with a delay of about 3...5 µS as compared with the clearing pulse (SO, MSO) with a defined flat loading edge. The rise time is about 6...10 µS (line). This relatively flat edge causes fewer disturbances on the lines adjacent to the identification wire than a steeper pulse edge. The flatting of the edge is brought about by the capacitor C21 between base and collector of switching transistor T16. The pulse length can be 85...100 µS at an amplitude of up to 2 Amp. At maximum resistance of the identification circuit the current must not be less than 450mA. As a transistor with a permissible collector current of 3 Amp is used as a switch, the pulse sender is largely immune to extraneous potentials of -60 V.

To protect the transistor T16 from cut-off voltages from the transformer, two diodes (G91, G92) have been connected in parallel with the transformer primary. (two diodes in series attenuate less than one diode).

Resistor R55 serves as a current limiter in the case of faults, i.e. if a transistor switches in quick succession (oscillates). The secondary winding of transformer L1 has a tapping to enable the pulse amplitude to be reduced if a lower range is required. The lower range (soldering pin 3) is about 60 Ω, the upper range (soldering pin 4) about 100 Ω.

A secondary winding (1,2) in series with the pulse winding (1,3,4) allows the reference potential to be raised by about 50 V (± 4,5 V) with respect to ground. In both secondary circuits only the positive half-cycle is used. The negative half-cycle is cut off by diode G45. The filter capacitor C10 which prevents the pulse sender from oscillating has been provided to stabilize the voltage supply of the pulse sender.

1.2.2 Identification pulse switch:

Component M8/T14 prevents ground being continuously applied to the identification wire ID1 or ID2 via the secondary winding(s). Transistor T14 is switched only if the identification pulse is sent. The switching time of this transistor exceeds the length of the identification pulse by about 5...10 µS. For a period of about 100 µS, the ground potential cannot interfere with the relays connected to the identification wire in the conventional switching system.

1.2.3 Control:

The control for the entire identifier consists of a common program control section (another card in this system) and of up to three identical steer in circuits (also another card in system) of which each is assigned a certain function. The common control section receives the seizure potential, determines the pulse times to be set, transmits the identification pulse and initiates the start of the individual steering circuits.

1.2.4 Seizure:

The seizure wire C of the identifier is protected from noise voltages by an RC network and a diode. Furthermore an operating threshold is provided by a zener diode. To ensure that the identifier starts reliably, the current flowing in the seizure wire C must exceed 5 mA. If less than 3,5 mA flow, the request remains ineffectual. In the case of a seizure from an external pulse generator, input CT is provided for test and measuring purposes (voltage at input CT about -10V). This input threshold (T1, C1, G1, G3) is followed by a delay network. (T2, T3, C2, R9) whose time delay can be gradually adjusted to between 800 µs and about 3 ms. This delay circuit is intended to gate possible noise pulses which may be produced by bouncing seizure contacts. Only if the request exceeds the selected delay time, is the identifier started with the aid of a pulse (M1/T20) via transistor T8. After the reception of the seizure signal, the equipment initiating the seizure (a ground potential) via wire Q for as long as the seizure condition exists (indicating a seizure acknowledgment signal). This ground potential blocks all other requesting devices. If ground potential is present on wire Q before the seizure, no seizure can take place. If the identification process has been completed, a respective criterion is sent over wire K (ground potential) indicating that the result can be accepted.

1.2.5 TIME-OUT FEATURE:

With the seizure of the identifier, a time-out feature (T9, T12, T13) is started. This feature operates if the seizure has not been removed after a time of about 6 mS to about 350 mS determined by resistor R31 has elapsed. The time-out feature must be set so that it does not operate during the normal seizure period, i.e. the supervisory time of the time-out feature must exceed the seizure time delay plus the first and second program run (identification process), the set time of the timing circuit (T17, T18, T19, T28) and, in the case of a fault, the repetition of the first and second identification process. The circuit design of this time-out feature is similar to that of the timing circuit described next which determines the delay between the first and second identification process.

1.2.6 TIMING CIRCUIT:

The timing circuit (T17, T18, T19, T28) for the intervals between the individual identification process can be adjusted within the range of about 200 µS to about 15 mS. This time is rather long compared to the normal pulse length of about 50 µS where the timing circuit uses no MT-components. A pulse of at least 8 µS discharges the capacitor C23 and causes the transistor T19 to conduct, a state which is retained until the transistor is cut off again via a Schmitt trigger when the capacitor has reached a certain charge. After this adjustable time (R62), the MT-component (T14, T28) connected in series, produces a pulse which initiates the starting of the succeeding selected program chain.

1.2.7 MAGNETIC-CORE TRANSISTOR RELAY COMPONENT (MT-COMPONENT):

Magnetic-core transistor relay components are mainly used to generate the control pulses. The MT-component is a circuit combination consisting of magnetic ring cores and a transistor whose base section is triggered by a winding of a ring core. The windings are of such polarities that it turns the transistor on when the set core ("0"-state) is interrogated. 40 Turns result in a pulse length of about 50 µS and 25 turns in a pulse length of 30 µS.

In the case of MT-cores interrogating other MT cores it is necessary for the interrogating pulse to be longer than the switching time of the core to be interrogated. The interrogating currents must be kept as low as possible to prevent time overlapping in the case of unfavourable tolerances.

Feedback enables an MT-component to be interrogated completely and at the same time a longer output pulse to be obtained. The output current of the transistor in the conducting state is used to interrogate the local core. In this way the core is interrogated completely even if the original interrogated pulse no longer exists. To prevent a noise pulse from switching this relatively sensitive component into the conducting state, an RC-network and a zener diode are switched into the interrogation circuit of this core to act as a threshold. This ensures that noise pulses of a length of up to 2 µS are safely prevented from switching the feedback core whereas a pulse of more than 5 µS reliably operates the component.

If the core of the MT-component is not set, it produces a short noise signal of about 2,5 µS on interrogation. In order to eliminate these noise pulses, ground potential is applied to the transistor only 4 to 5 µS after the interrogation has started. Here again, an MT-component is used as a timing circuit which utilizes the abovementioned noise pulse. A potentiometer connected to the base circuit of the transistor allows the switching time of the core and thus the pulse length to be continuously varied from about 2 to 8 µS or, about 11 to 35 µS. Due to the resistor, the secondary circuit of the component is loaded less and the core returns to the "0" state more quickly.

The time for the clearing pulse (SO, MSO), the setting time of the subscriber core (S1X, S1Z) and the length of the error checking pulse (CP) are set in this way.

All timing components are accommodated on the central plug-in-units. All the times are selected centrally for the three programs and limit the relevant clock pulses of varying lengths produced by the program chains. Pulses used for the clearing of the cores (SO, MSO) and for the interrogation of the hundreds group cores are heavily loaded in the case of large capacity identifiers. For this reason, the pulses on the various modules are converted with the aid of driving circuits which in turn, interrogate the cores.

1.2.8 IDENTIFICATION PULSE SUPERVISORY CIRCUIT:

The identification pulse is checked with the magnetic core thyristor component M9/T15. The magnetic core is controlled in the direction of the "1" state by pulse S1X which determines the setting time for the subscriber cores. This checking pulse is then compensated by the identification pulse.

The compensation winding which represents a shunt, is split into parallel branches. Similar to the circuit of the watt meter, a voltage measurement is carried out in one branch and a current measurement in the other so that the compensation of the checking pulse S1X is unaffected by the load of the pulse generator.

1.2.9 COMPONENT DESCRIPTION OF IDENTIFIER CARD:

M1/T20/T21	Starting pulse after seizure / Stop pulse after the completion of the seizure.
M2/T22	Generation of the clearing pulse SO.
M3/T23	Pulse of about 5 µS to eliminate noise pulse on interrogation.
M4/T24	Generation of the adjustable clearing pulse SO.
M5/T25	Generation of the starting pulse S12 for the current program.
M6/T26	Pulse of about 5 µS to eliminate the noise pulses.
M7/T27	Generation of the adjustable starting pulse S1X....the length of this pulse determines the setting time of the subscriber cores (identification pulse).
M8/T14	Central switch for identification pulse...the identification wire ID1 or ID2 must be free from potential in the non-operating condition (ground via solder terminal II2 or II3)
M9/T15	Supervisory component for the identification pulse. T15 is fired by pulse S1X if the identification pulse is absent. Switching principle is similar to watt meter circuit, i.e. current (G49) and voltage measurement (G50).
M10/T16	Generation of the identification pulse. The identification pulse can be transmitted super-imposed with respect to ground or about +50 V.

M11	Delay core for the elimination of noise pulses of T5, generated on interrogation of the magnetic core M12 which is retained in the "1" state (seizure) in order to prevent the succeeding magnetic core/thyristor component from being fired erroneously.
M12/T5	Detection of a short seizure, i.e. the seizure has been removed prior to the last program pass (see M11).
M13/T6/T7	End-of-program signal. It cuts off transistor T8. The ground remains at wire Q (G15).
M14/T28	Program starting pulse after the time set by R62 has elapsed.
M15/T31/M16 T32/M17/T33	Components for the generation of the checking pulses.
M18/T34	Auxiliary component for relay storage of visual display. T34 is preparatively fired and continues to hold the preceding internal seizures. The identifier is thus barred from further seizures and the relays can store the identification result.
T1/T2	Seizure.
T3/C2/R9	Seizure timing circuit. To eliminate noise pulses (e.g. bouncing relay contact) on the seizure wire C or CT. A seizure is accepted via the identifier only after this adjustable time has elapsed (T8).
T4	Switch for T3.
T8	Seizure received.
T9/C6/R31	Seizure time supervision.
T12/T13	Alarm. Seizure lasts longer than time set by R31.
T10/T11	Identifier is seized (PC) or not seized (NS).
T17/C23/R62 T18/T19	Timing circuit for the interval between two identification processes. This time must be set as the particular case requires, e.g. if the identification was carried out via RC networks or if the identification wires are shorted for varying lengths of time due to selector overflow.

T29/T30	Together with M1/T20 cancelling pulse for the display module on wire 1 at the following times: (a) at the beginning and (b) after the end of the seizure, if necessary by key.
G1, G2	Decoupling diodes.
G3	Zener diode for voltage stabilization.
G4...G6	Decoupling diodes.
G7	Zener diode together with G6 (attenuation of G7) for voltage stabilization at C2.
G8	Access diode to improve switching of T4.
G9/G10	Decoupling diodes.
G11	Rectifier to protect the base-emitter path of T5.
G12...G22	Decoupling diodes.
G23/G24	Diodes to improve switching of T8.
G25...G27	Decoupling diodes.
G28, G29	Switching diode for T10 or T9.
G30	Decoupling diode.
G31	Zener diode for voltage stabilization. It also improves switching of T9.
G32	Decoupling diode.
G33, G40, G39, G43	Protective rectifier.
G34, G35	Switching diodes for T11.
G36...G38	Decoupling diodes.
G41, G42	Switching diodes for T13.
G44, G46, G47	Protective rectifier of T14.
G45	Decoupling diode.

G48	Zener diode for voltage limitation of T14.
G49, G55	Protective diodes to prevent T15 from being erroneously fired by noise pulses.
G56	Zener diode as operating threshold of timing circuit (T17).
G57, G59, G61, G60, G64...G67, G71	Decoupling diodes.
G58	Switching diode of T18.
G62	Protective rectifier of T28.
G68...G70	Switching diodes of T30.
G72...G77	Protective rectifiers for the base-emittor paths.
G78...G82	Decoupling diodes.
G83...G85	Protective rectifiers for the base-emitter paths.
G86...G90	Decoupling diodes.
G91, G92	Protective diodes against erroneous firing due to noise pulses.
G103...G105	Decoupling diodes.

1.3 DESIGN CONSIDERATIONS:

The ID tester is designed to meet the following specifications:

* The tester must be easy to operate (No driver licence required).
* The material cost must be as low as possible (all components from National Electronic Repair Centre's store).
* The tester must operate from mains.
* The tester must indicate a fault or faults as clear as possible (easy to interpret).
* The test must run continuously so that it is easy to trace on a oscilloscope etc.
* If the tester goes faulty, it must be easy to repair by any technician.

2.0 DESIGN IMPLEMENTATION:

The ID tester was designed on purely a hardware basis with no software involved. A processor could be used in the design, but with the available hardware available, it wasn't necessary.

2.1 BLOCK DIAGRAM OF IDENTIFIER CARD TESTER:

See figure 2.1.1 (Identifier card tester) and figure 2.1.2 for the block diagram of the Identifier card tester.

2.1.1 BASIC DESCRIPTION OF THE BLOCK DIAGRAM:

This Tester consists of the following modules;

1.0	Timing Module	(one of)
2.0	Pulse Sender Module	(one of)
3.0	Driver Interface Module	(two of)
4.0	Display Interface Module	(two of)
5.0	Comparator Module	(one of)
6.0	Display Unit	(two of)
7.0	Power Module	(one of)

The Timing module generates all the pulses on this ID tester. These pulses are then transferred to the Pulse Sender module and the Driver Interface modules which then convert these pulses to the potentials accepted by the Reference cards etc.

The Display Interface modules will then convert the output signals of the cards to suite the Comparator module and the Display unit. The nineteen outputs of each Display Interface module will be transferred to the red led's via. a ribbon cable. The (Ref. & U.U.T) Cards work from -48 Volts, where the Tester functions on 5 Volts. The Comparator module will compare six outputs from each of the Display Interface modules and transfer the complement via Ribbon cable to the Display unit (six white Led's).

2.1.2 TEST STAGES:

By using a rotary switch you can select six different "test stages". These six stages divide the test procedure up into six smaller sections so that only certain pieces of the cards are being tested at a time. This function then also illuminates possible interferences from other sections. (This type of card is very suspectable to interferences due to the one winding of the coils (of the smaller sections) that are basically all connected to each other.) Without interference from the other smaller sections the technician can now more easily locate the faulty section and the faulty component.

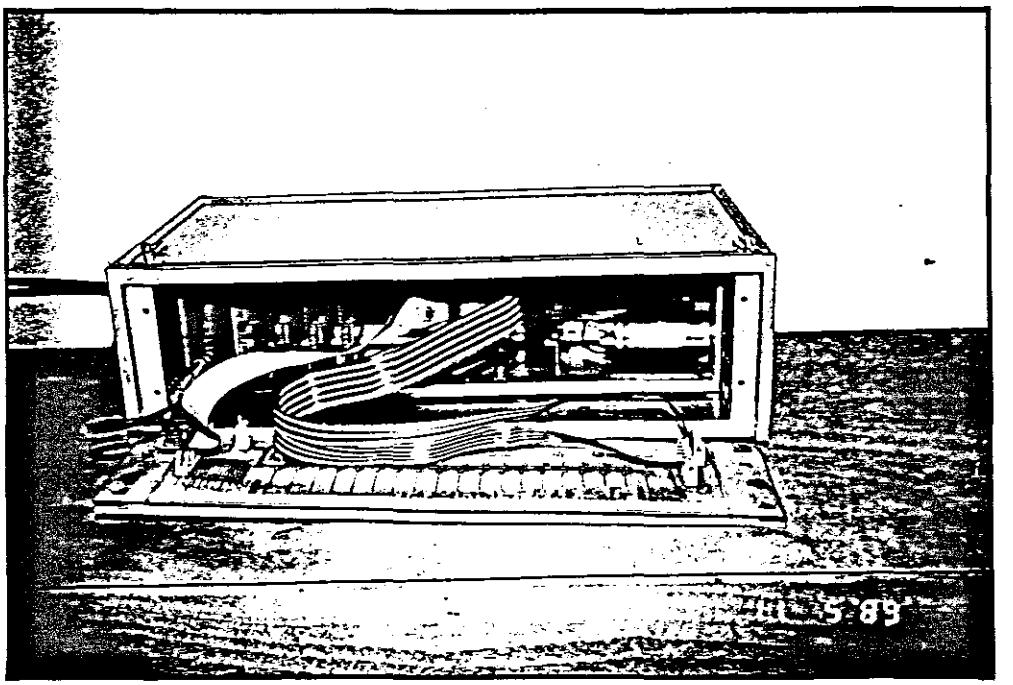


Fig 2.1.1 Identifier card tester with face plate unscrewed.

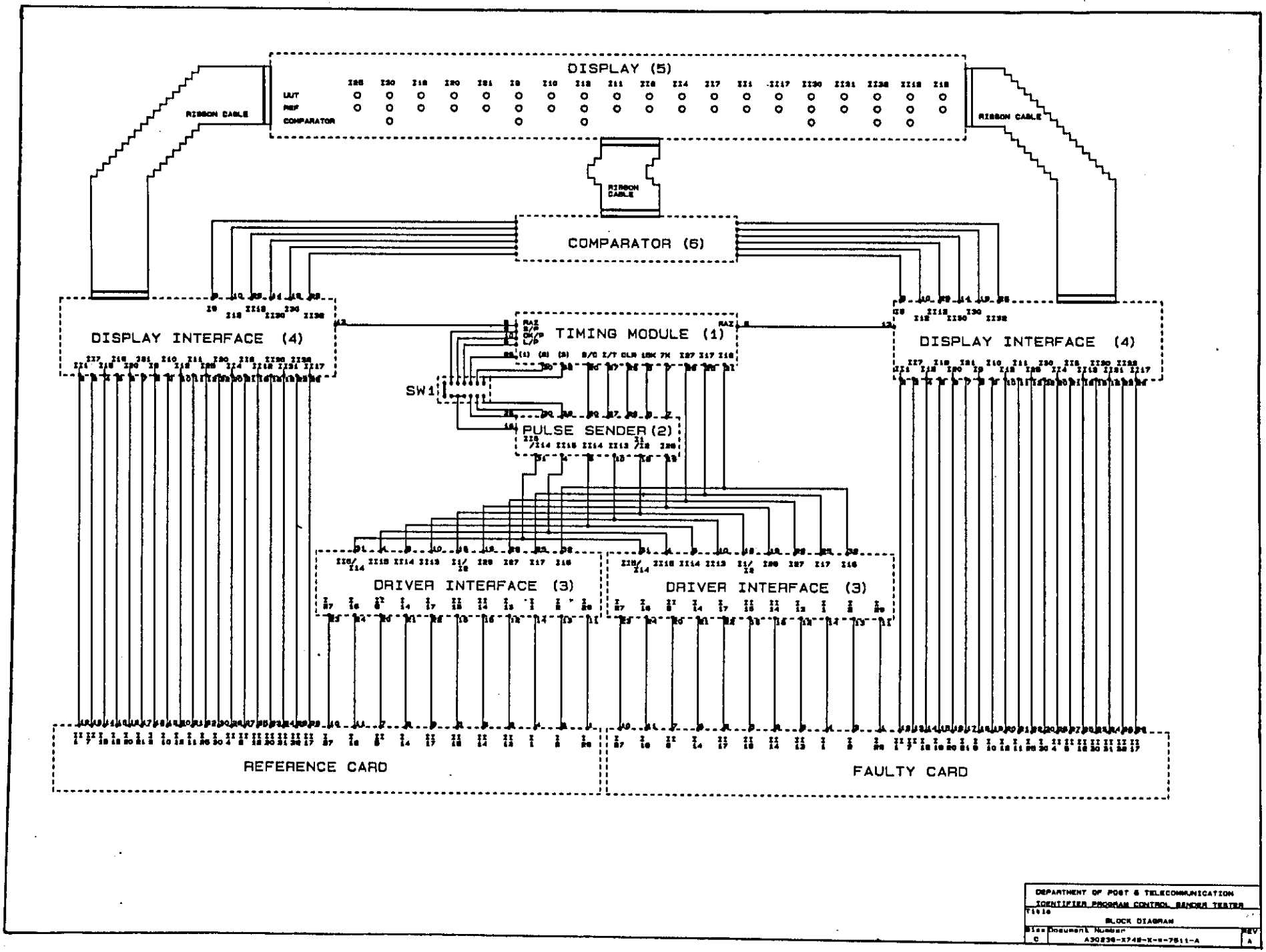


Fig 2.1.2 Block diagram of Identifier card tester.

Test Stages:

	inputs active									
Switch position	I1/I2	II5	I14	I17	II13	II14	II15	I16	I27	I29
1	No	Yes	Yes	Yes	No	No	No	Yes	Yes	Yes
2	Yes	Yes	Yes	Yes	No	No	No	Yes	Yes	Yes
3	Yes	Yes	Yes	Yes	No	No	No	Yes	Yes	Yes
4	Yes	Yes	Yes	Yes	No	No	No	Yes	Yes	Yes
5	No	Yes	Yes	Yes	Yes	No	No	Yes	Yes	Yes
6	No	Yes	Yes	Yes	No	Yes	No	Yes	Yes	Yes
7	No	Yes	Yes	Yes	No	No	Yes	Yes	Yes	Yes

2.2 TIMING MODULE:

2.2.1 CIRCUIT DESCRIPTION OF TIMING MODULE:

The basic function of the Timing module (fig 2.2.3) is to supply the relative pulses to the Pulse Sender module and the Driver module. These pulses are generated by a 8 MHz Resonator or Crystal clock (X1), the heart of the ID Tester. This Module makes provision for either a Resonator or a Crystal. When using a Crystal, IC12 must be a 7404 and when using a Resonator, IC12 must be a 74HC04 which has a higher input impedance than the 7404. The 8 MHz is then divided by using D-Type F/F's (IC10 and IC11) first and then two 12-stage dividers (IC7 and IC8). The input on pin 10 of IC7 will be 1 MHz which is then used to generated the specific timing pulses.

The inputs of IC6 (4/16 dec.) are 0,5 Hz; 1 Hz; 2 Hz and 4 Hz, giving an output of 500 msec, every 4 seconds on one of its outputs. By using 3- and 4-input Nand gates the Module generates the following pulses.

1.0	RAZ pulse	64 µS - every one sec.
2.0	15 KHz	15 KHz.
3.0	7 KHz	7 KHz.
4.0	Too short (Seizure)	250 Hz.
5.0	OK (Seizure pulse)	63 Hz.
6.0	Too long (Seizure)	1 Hz.
7.0	Seizure (Select/Clear)	1sec. every 4sec.
8.0	[1] Checking pulse	250 mS every 4sec.
9.0	I27 Cancelling pulse	750 mS every 4sec.
10.0	[2] Checking pulse	250 mS every 4sec.
11.0	I17 Aux. storage	250 mS every 4sec.
12.0	Interval timer	250 mS every 4sec.
13.0	[3] Checking pulse	250 mS every 4sec.
14.0	I16 Cancelling pulse	750 mS every 4sec.
15.0	RAZ/CLEAR	250 mS every 4sec.

The Timing module is reset every 4 seconds by output pin 15 of IC8, combined with IC12e, IC9c and IC12f. This means that every 4 seconds the test procedure is restarted in the ID tester automatically.

R1 and C1 will generate a time delay when the tester is switched-on. This delay will make sure that the modules and cards are stabilized before the timing pulses arrive.

2.2.2 TIMING DIAGRAM OF THE TIMING MODULE:

See figure 2.2.2 for the output signals generated by the Timing module.

2.2.3 CIRCUIT DIAGRAM OF THE TIMING MODULE:

See figure 2.2.3 for the circuit diagram of the Timing module.

2.2.4 COMPONENT LIST:

RESISTORS:

R1	1 KΩ	¼ W
R2	4,7 KΩ	¼ W
R3	4,7 KΩ	¼ W
R4	4,7 KΩ	¼ W
R5	4,7 KΩ	¼ W
R6	4,7 KΩ	¼ W
R7	4,7 KΩ	¼ W
R8	4,7 KΩ	¼ W
R9	4,7 KΩ	¼ W
R10	4,7 KΩ	¼ W
R11	4,7 KΩ	¼ W
R12	1 KΩ	¼ W
R13	1 KΩ	¼ W
R14	100 KΩ	¼ W

CAPACITORS:

C1	1 µF	16V - Tan.
C2	56 pF	
C3	56 pF	

IC's:

IC 1	7407
IC 2	74LS20
IC 3	74LS10
IC 4	74LS30
IC 5	74LS30
IC 6	74LS154
IC 7	4040
IC 8	4040
IC 9	74LS00
IC 10	74LS74
IC 11	74LS74
IC 12	74HC04/7404

MISCELLANEOUS:

X 1	8 MHz Resonator/Crystal

2.2.5 PRINTED CIRCUIT BOARD LAYOUT:

See figure 2.2.5.1 for the silk screen layout, figure 2.2.5.2 for the component side layout and figure 2.2.5.3 for the solder side layout of the Timing module.

Fig 2.2.2 Timing diagram of Timing module.

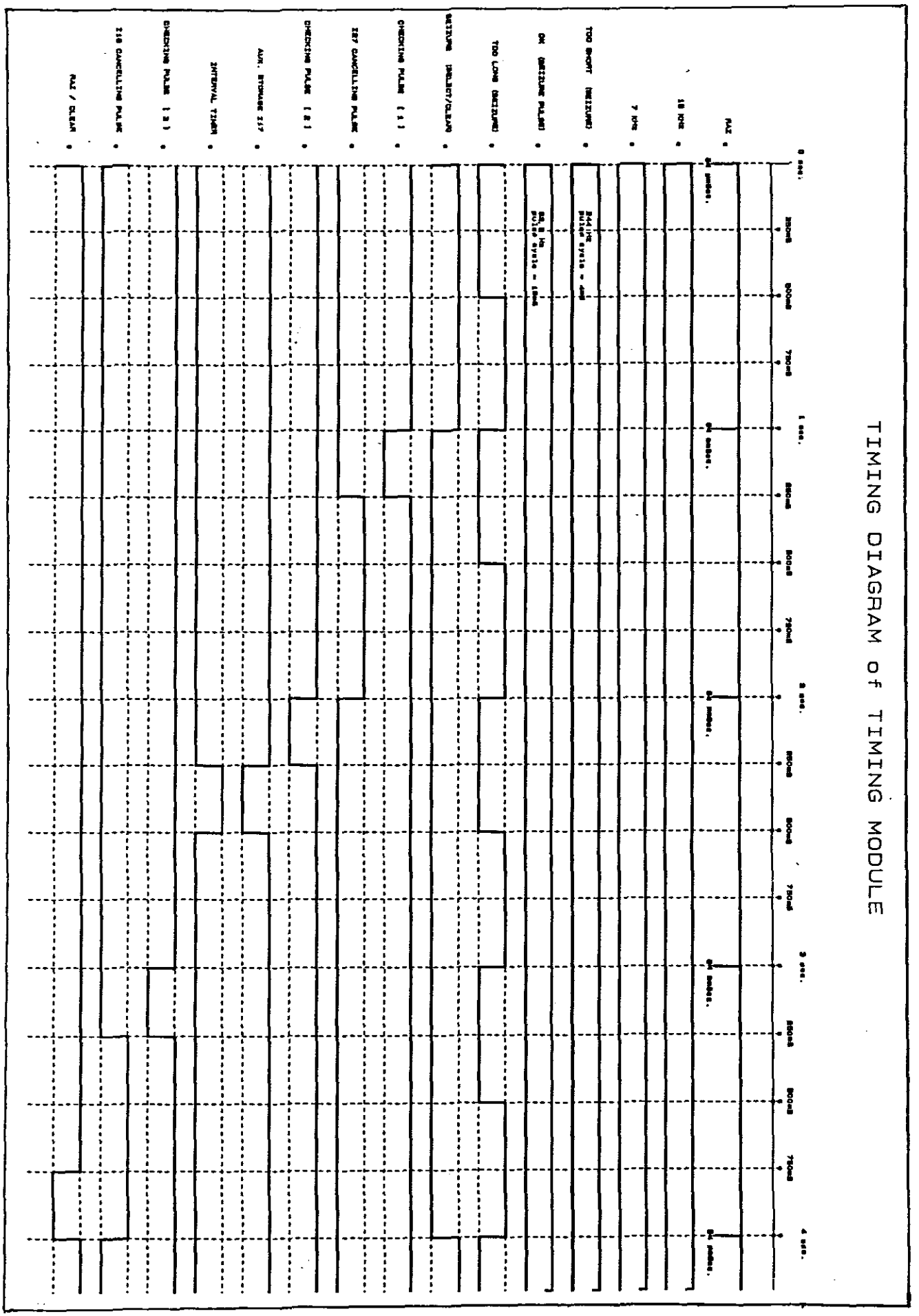
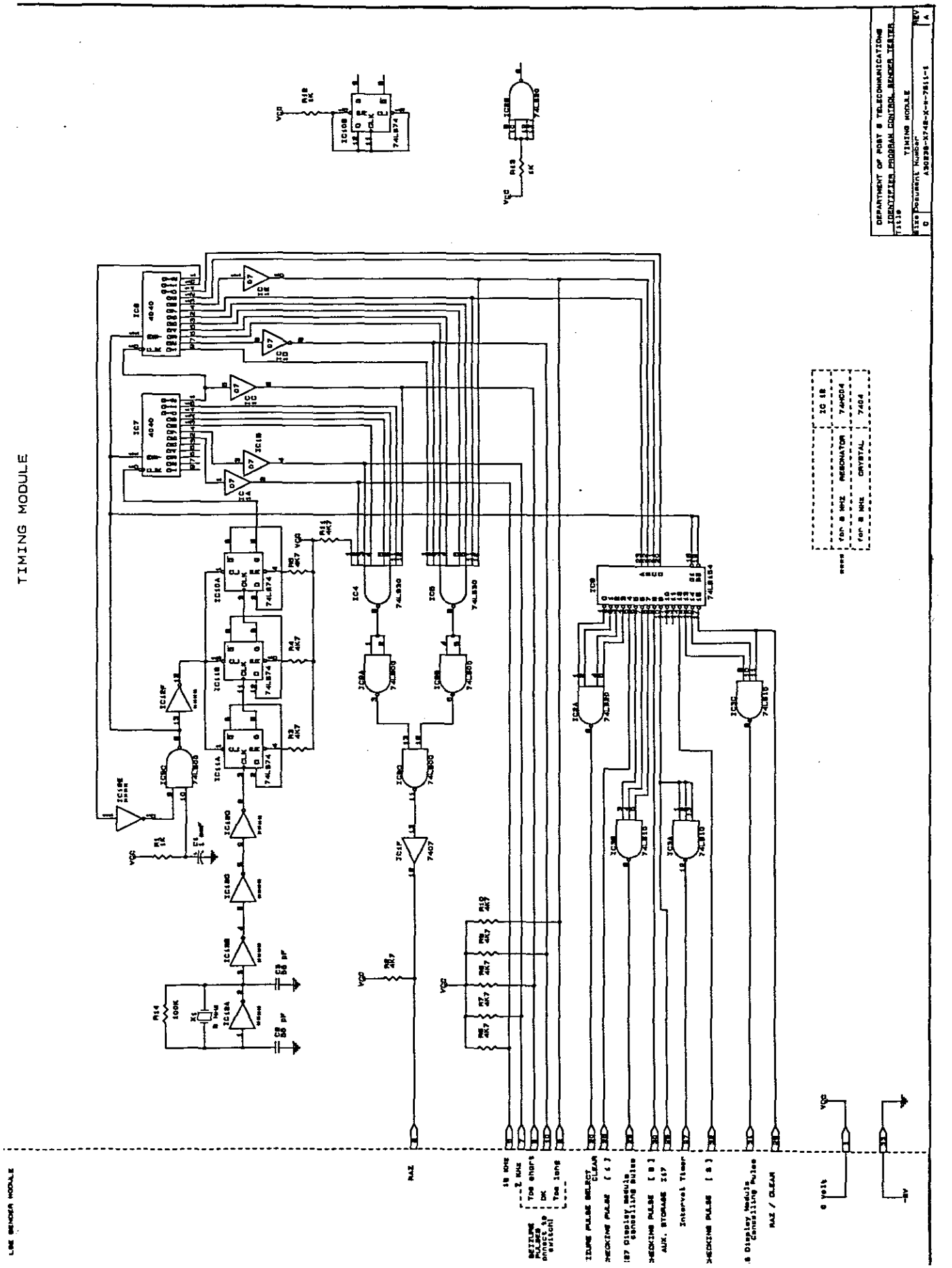


Fig 2.2.3 Circuit diagram of Timing module.



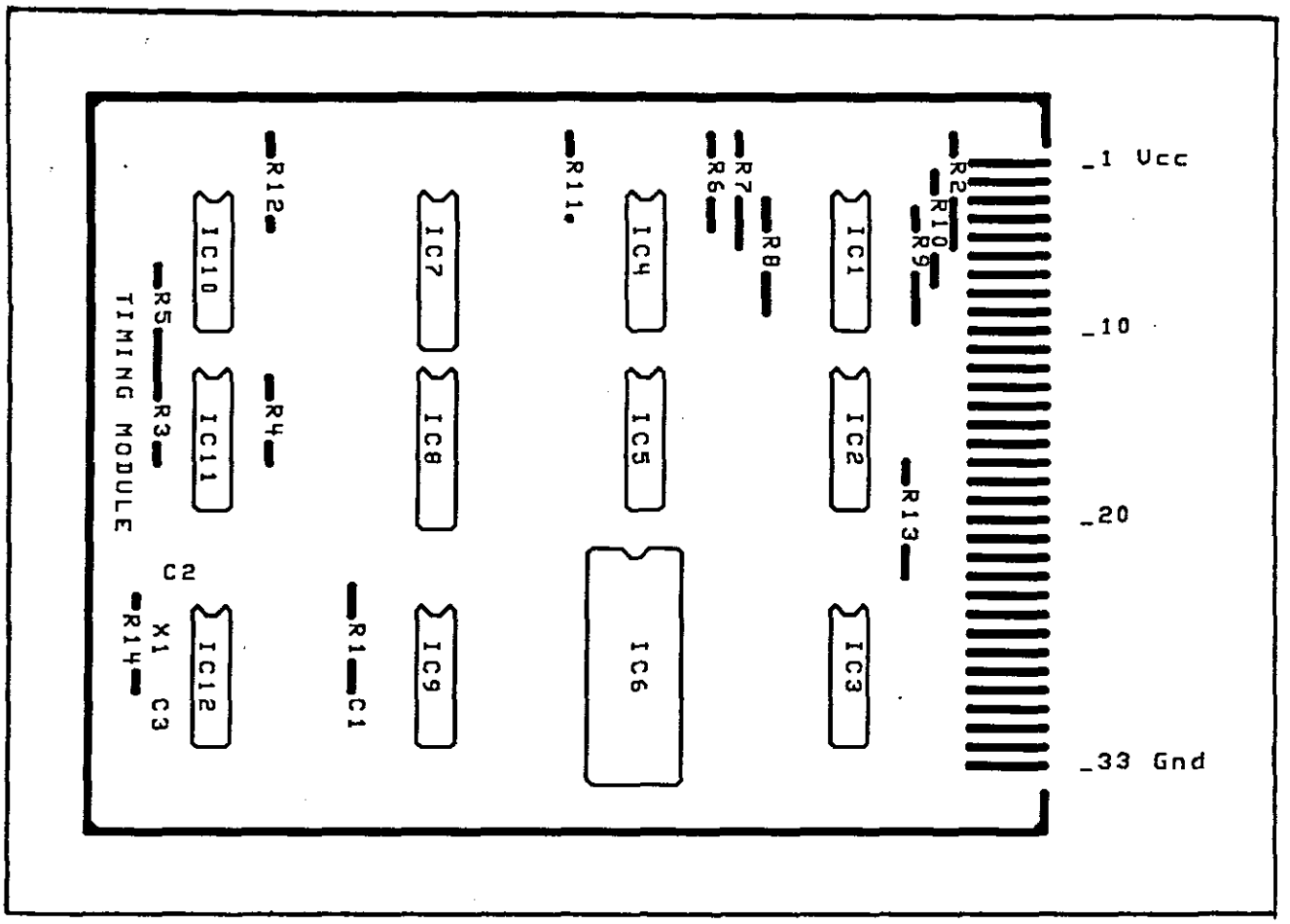


Fig 2.2.5.1 PC board layout (silk screen) of Timing module.

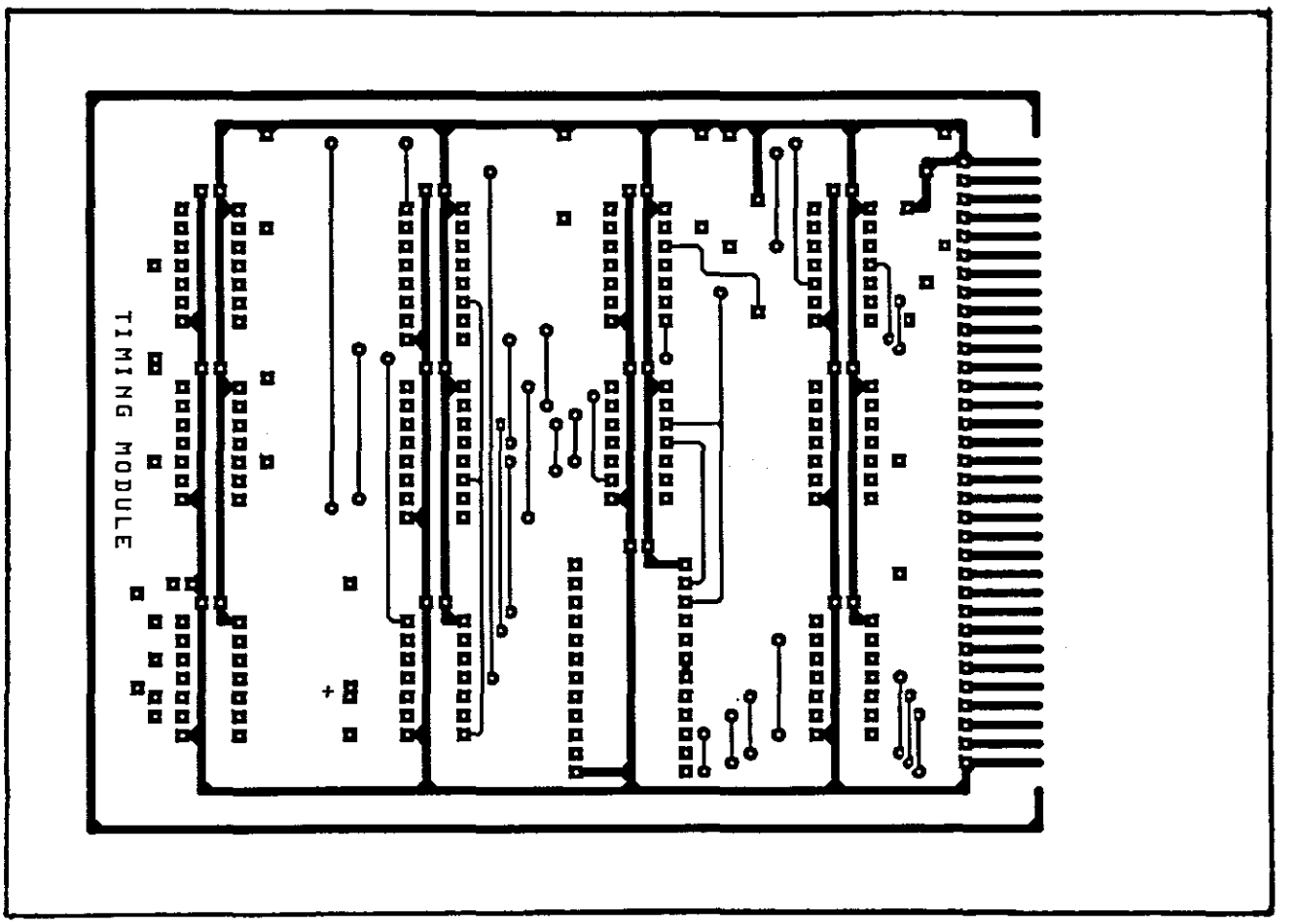


Fig 2.2.5.3 PC board layout (component side) of Timing module.

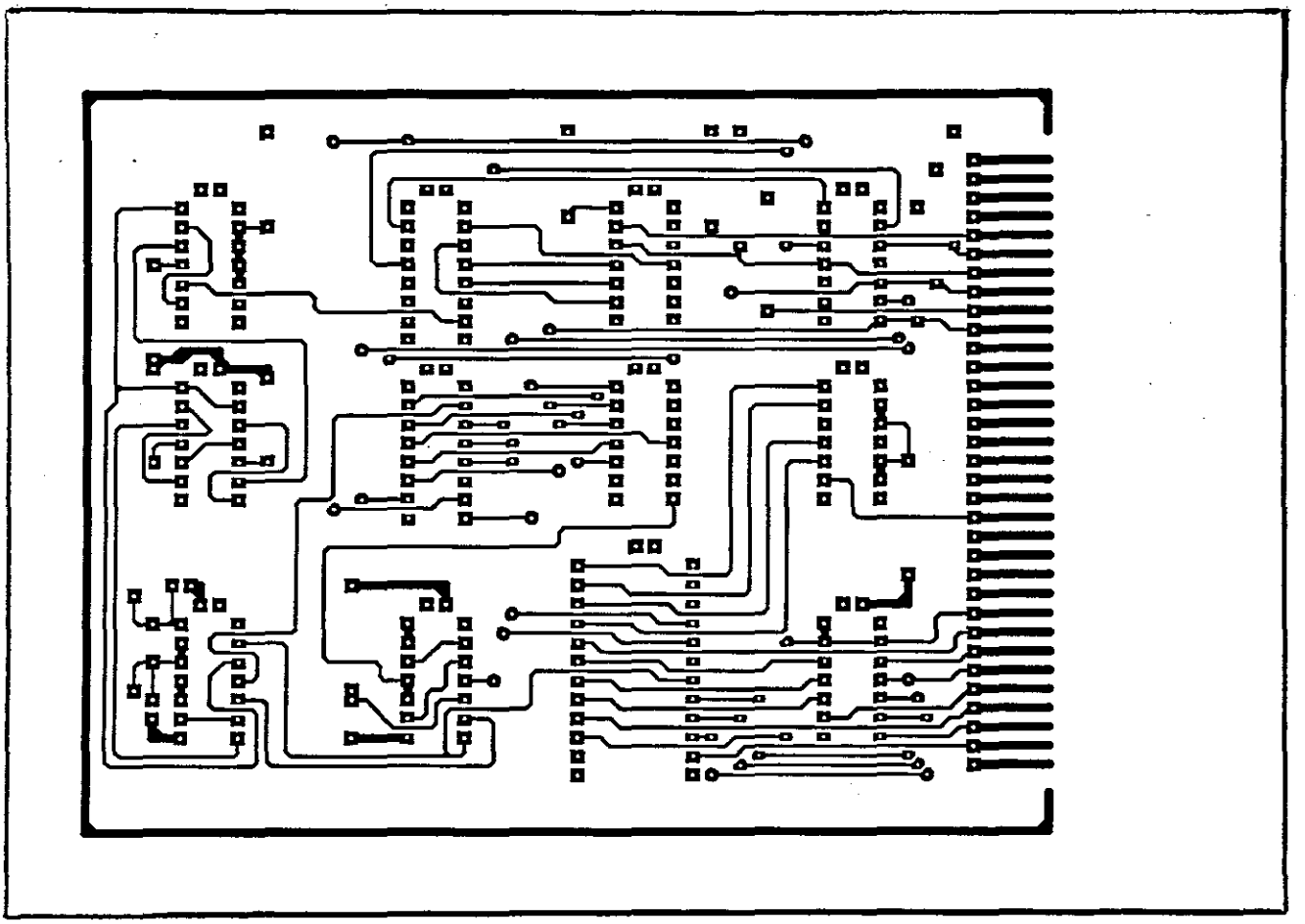


Fig 2.2.5.2 PC board layout (solder side) of Timing module.

2.3 PULSE SENDER MODULE:

2.3.1 CIRCUIT DESCRIPTION:

The basic function of this module (fig 2.3.2) is to combine some of the pulses from the Timing module and to generate pulses of a specific length.

On this module the pulses (RAZ/CLEAR ; [1] ; [2] & [3]) are given a higher power output so that they can drive more IC's (IC fanout).

You can select any one of the seizure pulses by means of a switch (position 2, 3 and 4). Switch position two will simulate a short seizure pulse of 2 mS, switch position three will simulate a pulse of 8 mS (normal seizure pulse) and switch position four will simulate a pulse of 500 mS (too long). The output signal of this switch is then combined with the pulse (Seizure Select/Clear) which is present for 1 second every cycle of 4 seconds. IC3 ,IC2d and IC1e will then generate one of the specified pulses selected by the switch, every 4 seconds.

A 15 KHz and a 1,5 second pulse every 4 seconds are also combined to generate a pulse of ± 60 μS every 4 seconds.

Timing plays a major role in testing the Identifier card and therefore you require only one pulse of a specific length in the testing cycle.

2.3.2 CIRCUIT DIAGRAM:

See figure 2.3.2 for the circuit diagram of the Pulse Sender module.

2.3.3 COMPONENT LIST:

RESISTORS:

R1	2,2 KΩ	¼ W
R2	2,2 KΩ	¼ W
R3	2,2 KΩ	¼ W
R4	2,2 KΩ	¼ W
R5	2,2 KΩ	¼ W
R6	2,2 KΩ	¼ W
R7	10 KΩ	¼ W
R8	10 KΩ	¼ W
R9	10 KΩ	¼ W
R10	10 KΩ	¼ W
R11	10 KΩ	¼ W
R12	10 KΩ	¼ W
R13	10 KΩ	¼ W
R14	10 KΩ	¼ W
R15	10 KΩ	¼ W
R16	10 KΩ	¼ W

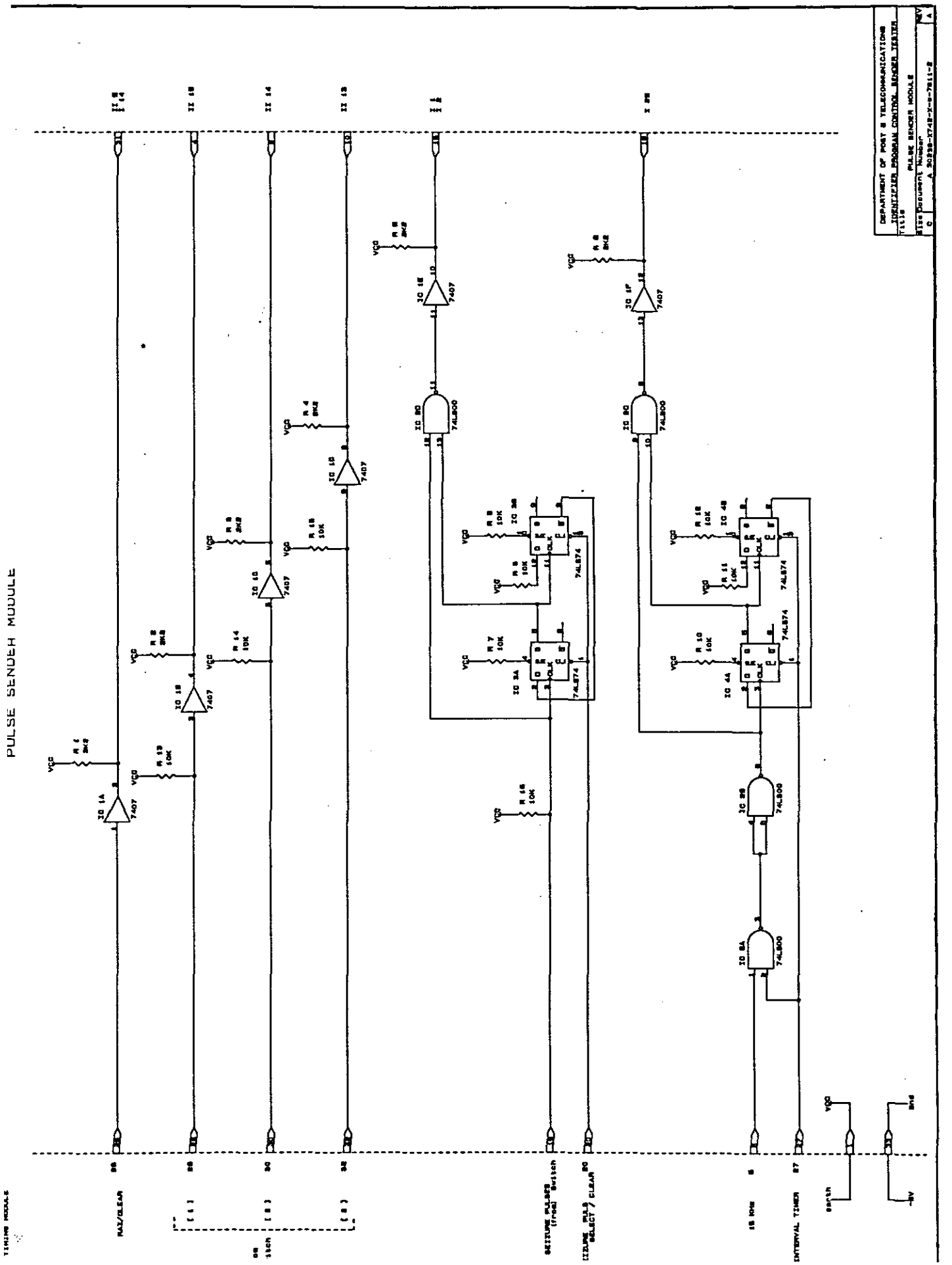
IC's:

IC 1	7407
IC 2	74LS00
IC 3	74LS74
IC 4	74LS74

2.3.4 PRINTED CIRCUIT BOARD LAYOUT:

See figure 2.3.4.1 for the silk screen layout, figure 2.3.4.2 for the component side layout and figure 2.3.4.3 for the solder side layout of the Pulse Sender module.

Fig 2.3.2 Circuit diagram of Pulse Sender module.



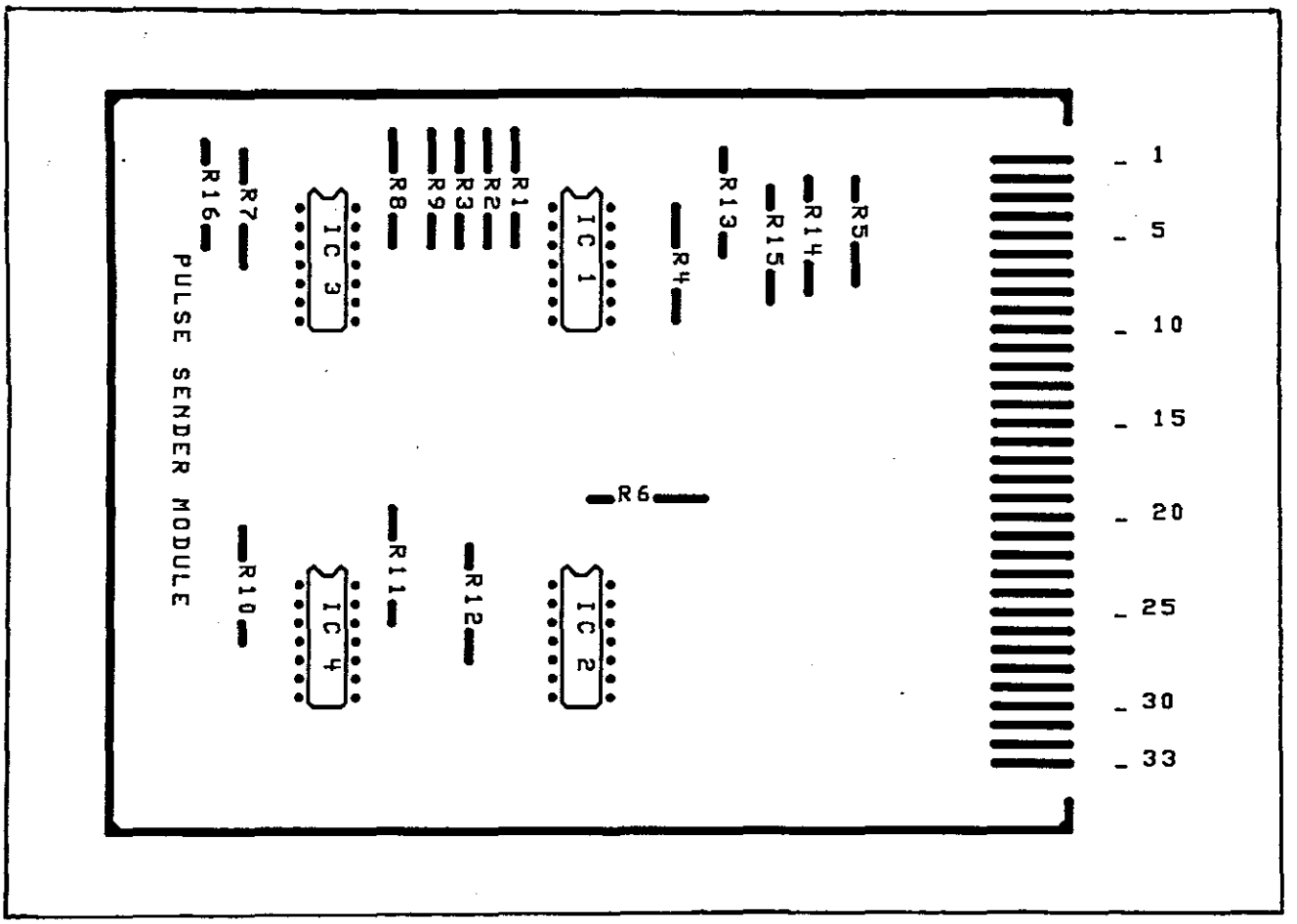


Fig 2.3.4.1 PC board layout (silk screen) of Pulse Sender module.

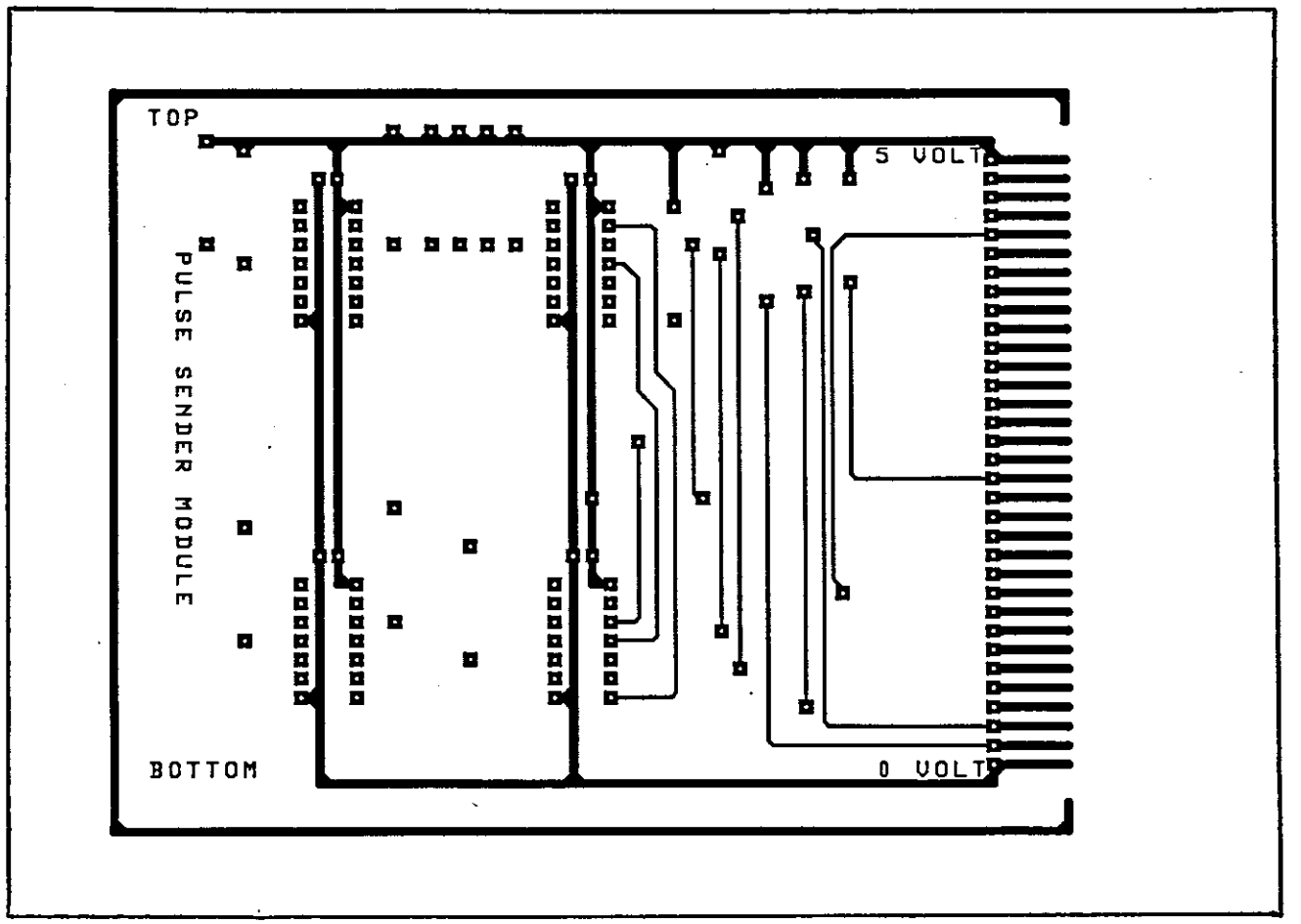


Fig 2.3.4.2 PC board layout (component side) of Pulse Sender module.

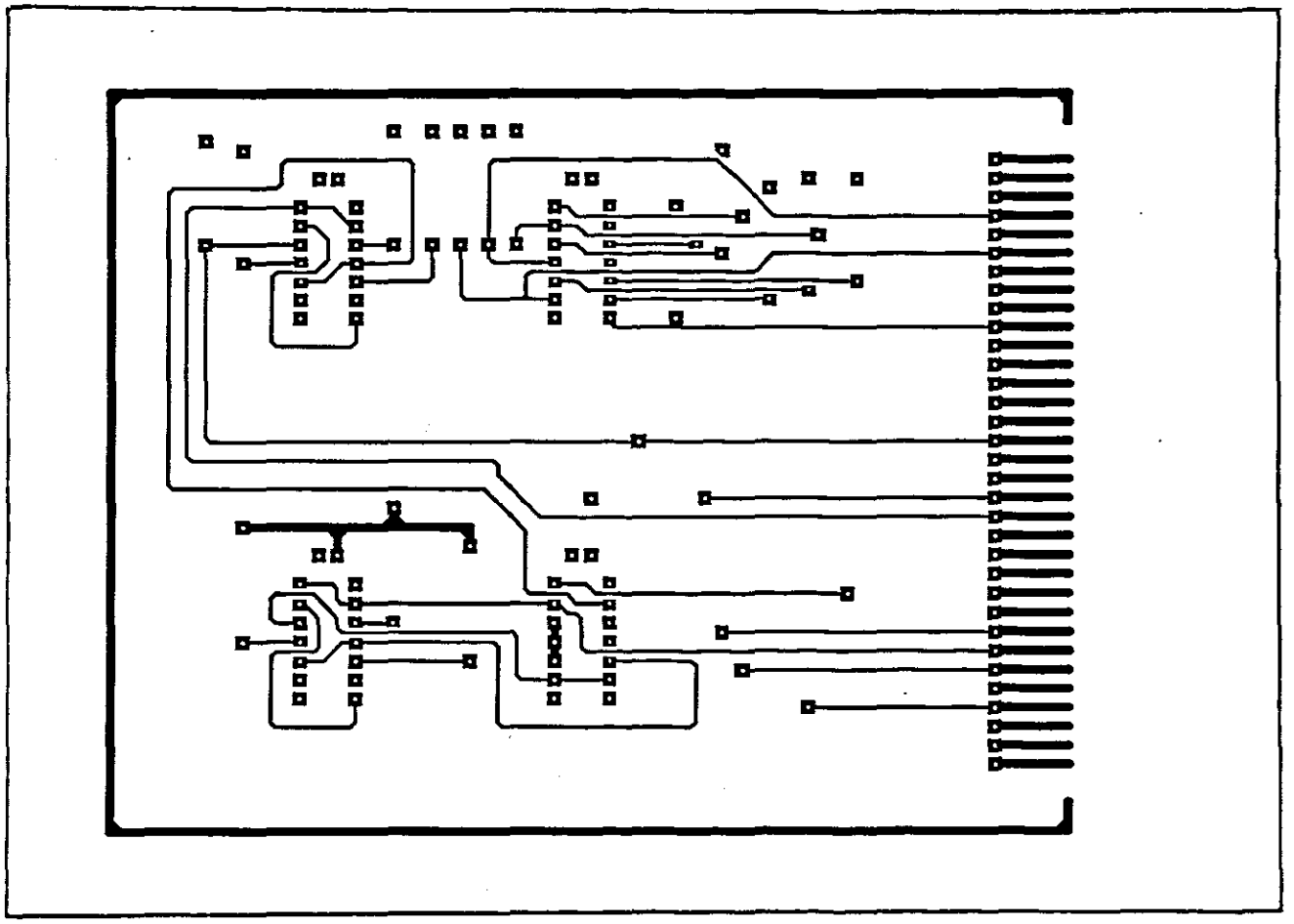


Fig 2.3.4.3 PC board layout (solder side) of Pulse Sender module.

2.4 DRIVER INTERFACE MODULE:

2.4.1 CIRCUIT DESCRIPTION:

The basic function of this module (fig 3.4.2) is to supply a interface between the 5 Volt of the tester and the 48 Volt of the card under test. All the pulses are send via opto couplers (SL5501). This module is also duplicated in the tester, one for the Unit Under Test and one for the Reference card.

IC10 and IC11 are Hex Buffers and Hex Inverter Buffers with open-collector outputs to drive the opto couplers (IC1 to IC9).

See figure 2.4.3 for the timing diagram on the output pulses going to the cards under test.

2.4.2 CIRCUIT DIAGRAM:

See figure 2.4.2 for the circuit diagram of the Driver Interface module.

2.4.3 TIMING DIAGRAM OF INPUT SIGNALS TO THE IDENTIFIER CARDS:

See figure 2.4.3 for the diagram of the output signals of the Driver Interface module to the Identifier cards.

2.4.4 COMPONENT LIST:

RESISTORS:

R1	4,7 KΩ	¼ W
R2	4,7 KΩ	¼ W
R3	4,7 KΩ	¼ W
R4	4,7 KΩ	¼ W
R5	4,7 KΩ	¼ W
R6	100 Ω	¼ W
R7	100 Ω	¼ W
R8	100 Ω	¼ W
R9	100 Ω	¼ W
R10	100 Ω	¼ W
R11	4,7 KΩ	¼ W
R12	4,7 KΩ	¼ W
R13	4,7 KΩ	¼ W
R14	4,7 KΩ	¼ W
R15	100 Ω	¼ W
R16	100 Ω	¼ W
R17	100 Ω	¼ W
R18	100 Ω	¼ W

IC's:

IC 1	SL5501
IC 2	SL5501
IC 3	SL5501
IC 4	SL5501
IC 5	SL5501
IC 6	SL5501
IC 7	SL5501
IC 8	SL5501
IC 9	SL5501
IC 10	7407
IC 11	7416

2.4.5 PRINTED CIRCUIT BOARD LAYOUT:

See figure 2.4.5.1 for the silk screen layout, figure 2.4.5.2 for the component side layout and figure 2.4.5.3 for the solder side layout of the Driver Interface module.

Fig 3.4.2 Circuit diagram of Driver Interface module.

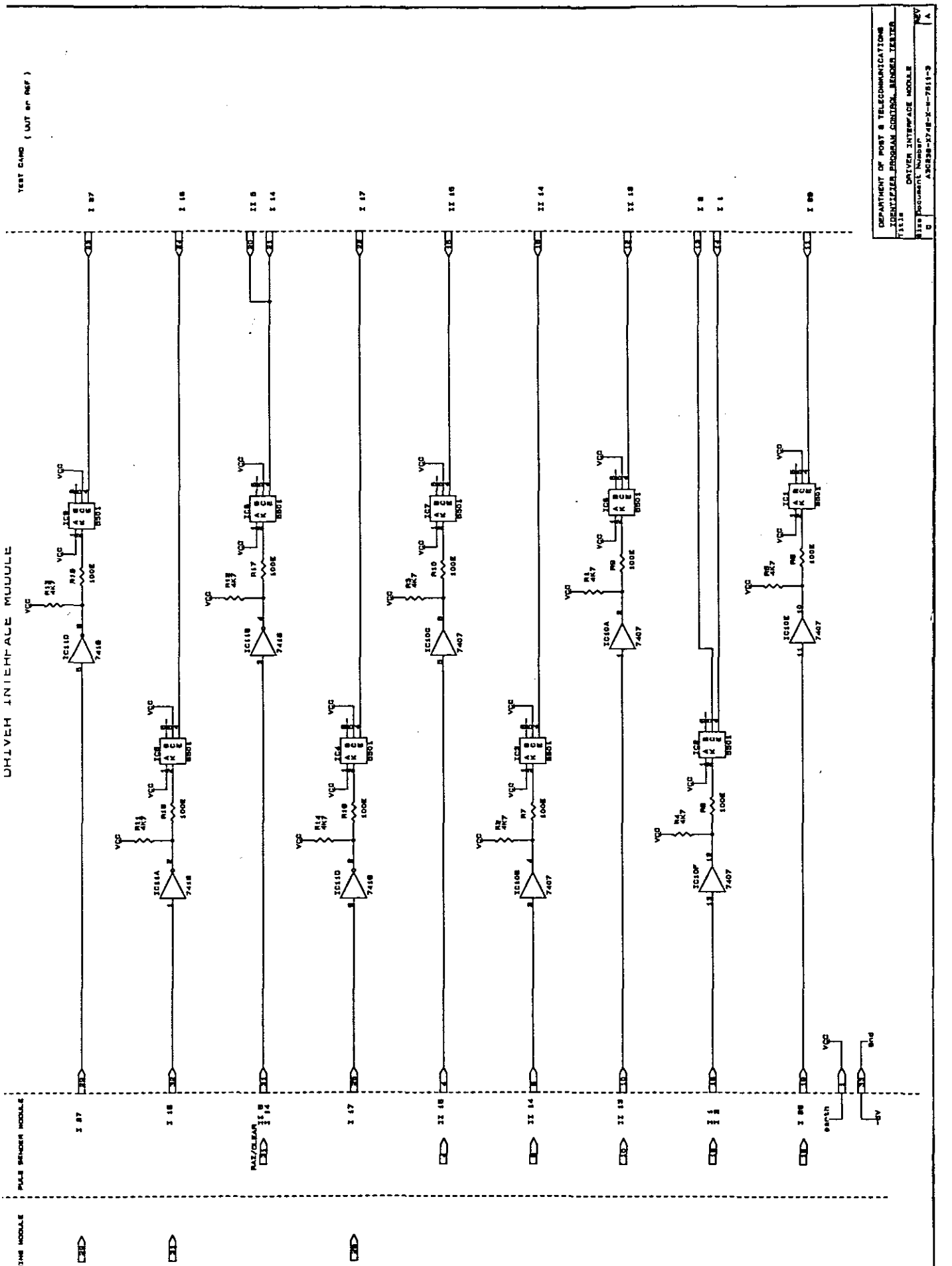
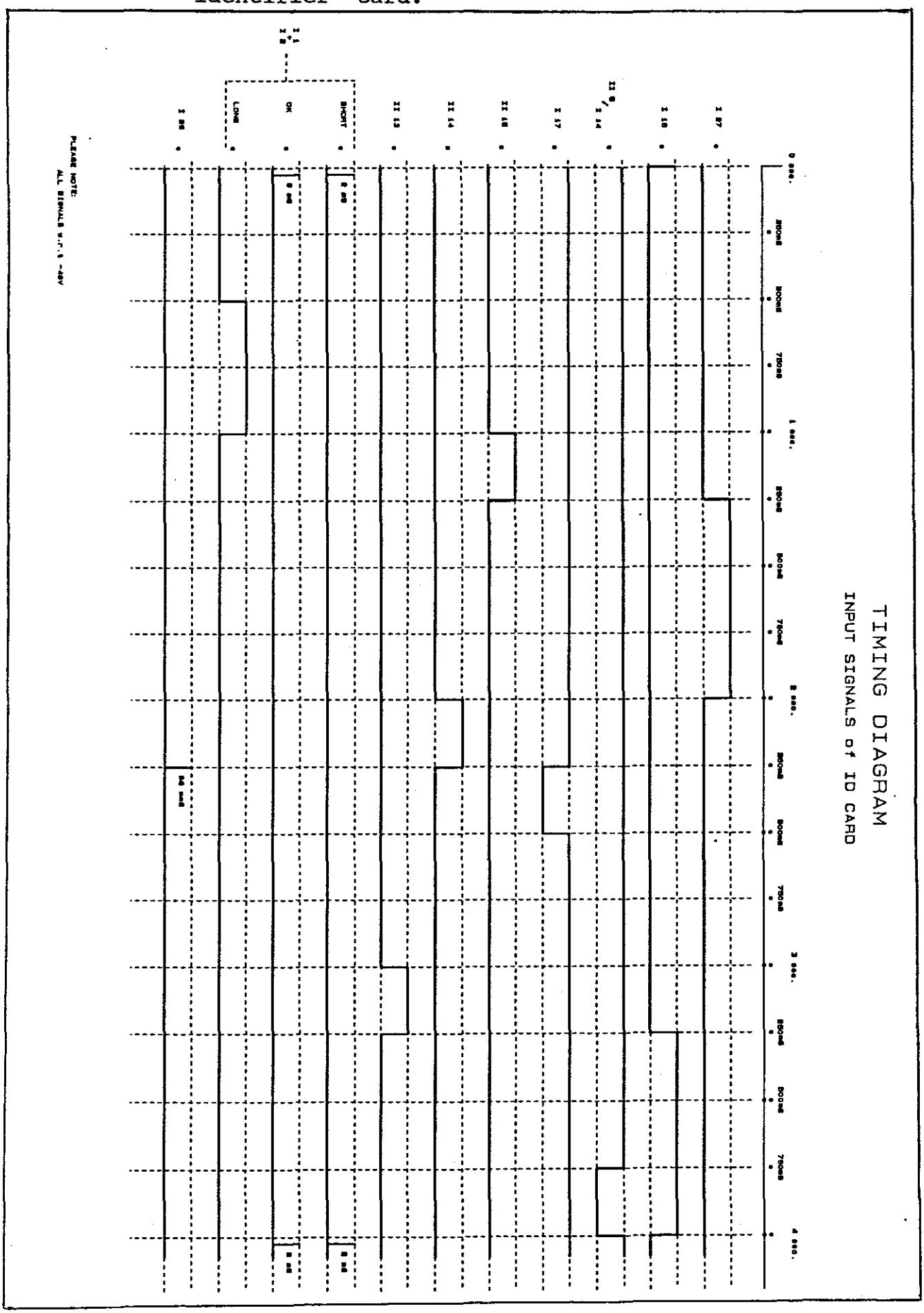


Fig 2.4.3 Timing diagram of the input signals to the "Identifier" card.



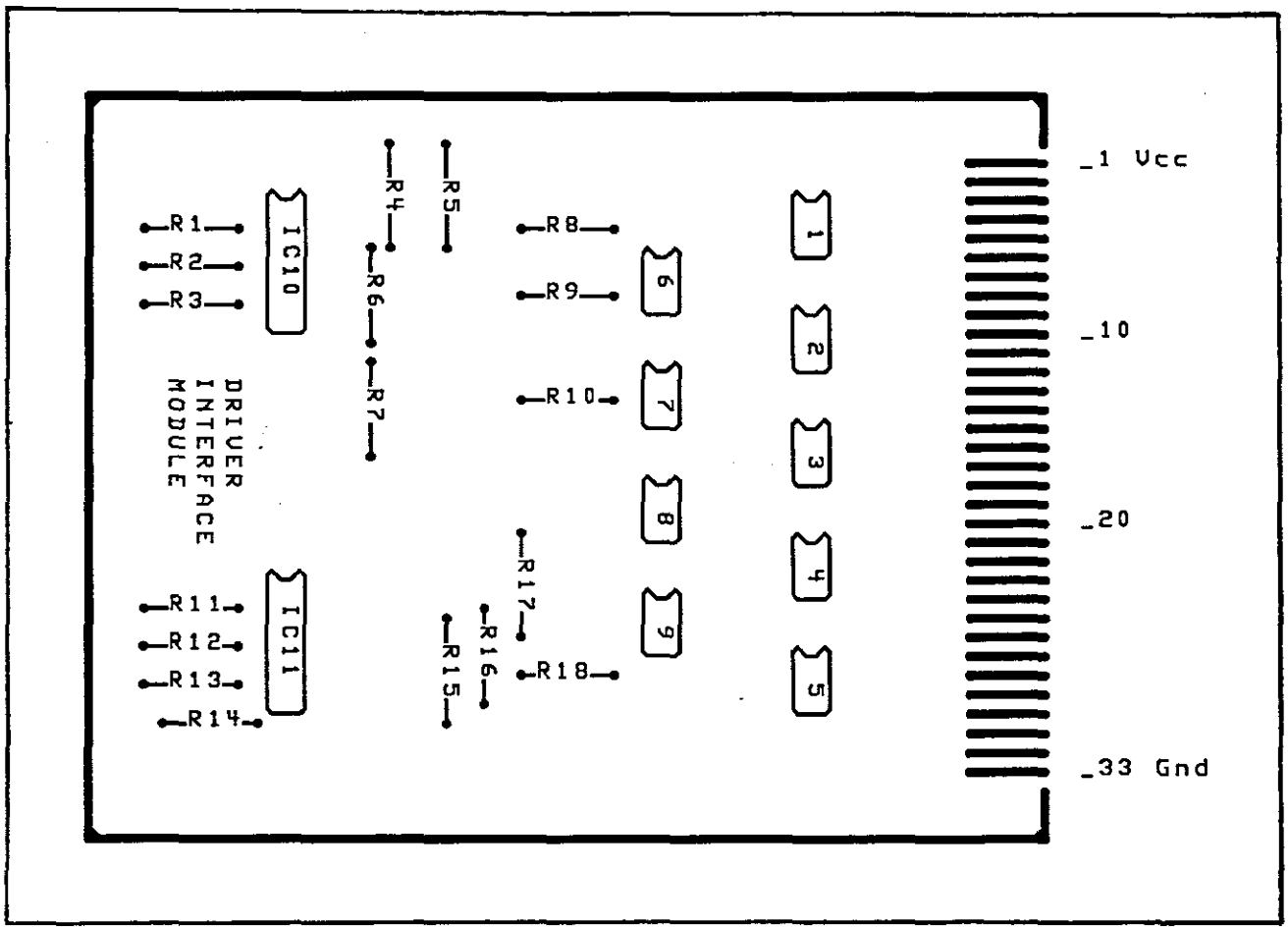


Fig 2.4.5.1 PC board layout (silk screen) of Driver Interface module.

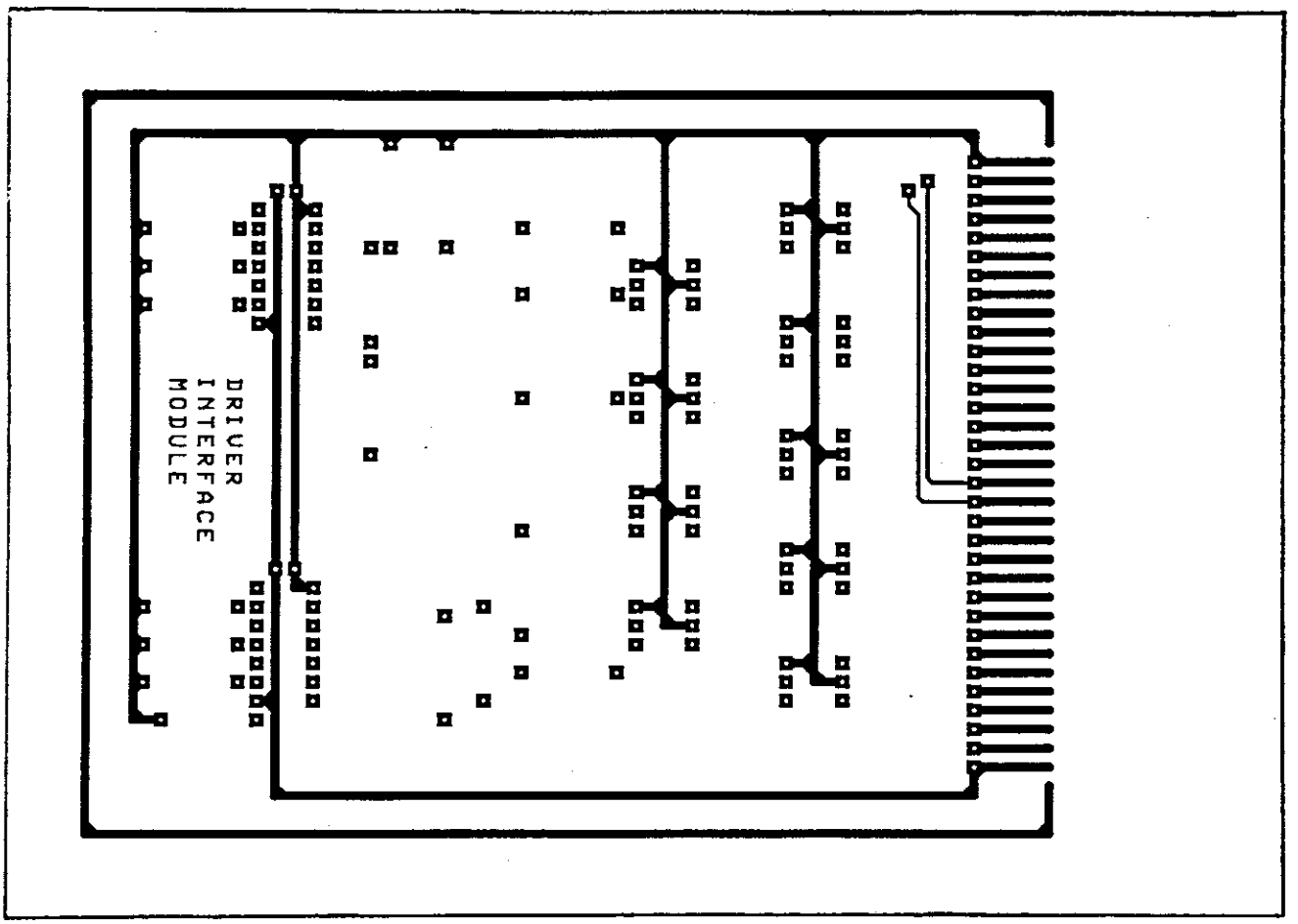


Fig 2.4.5.2 PC board layout (component side) of Driver Interface module.

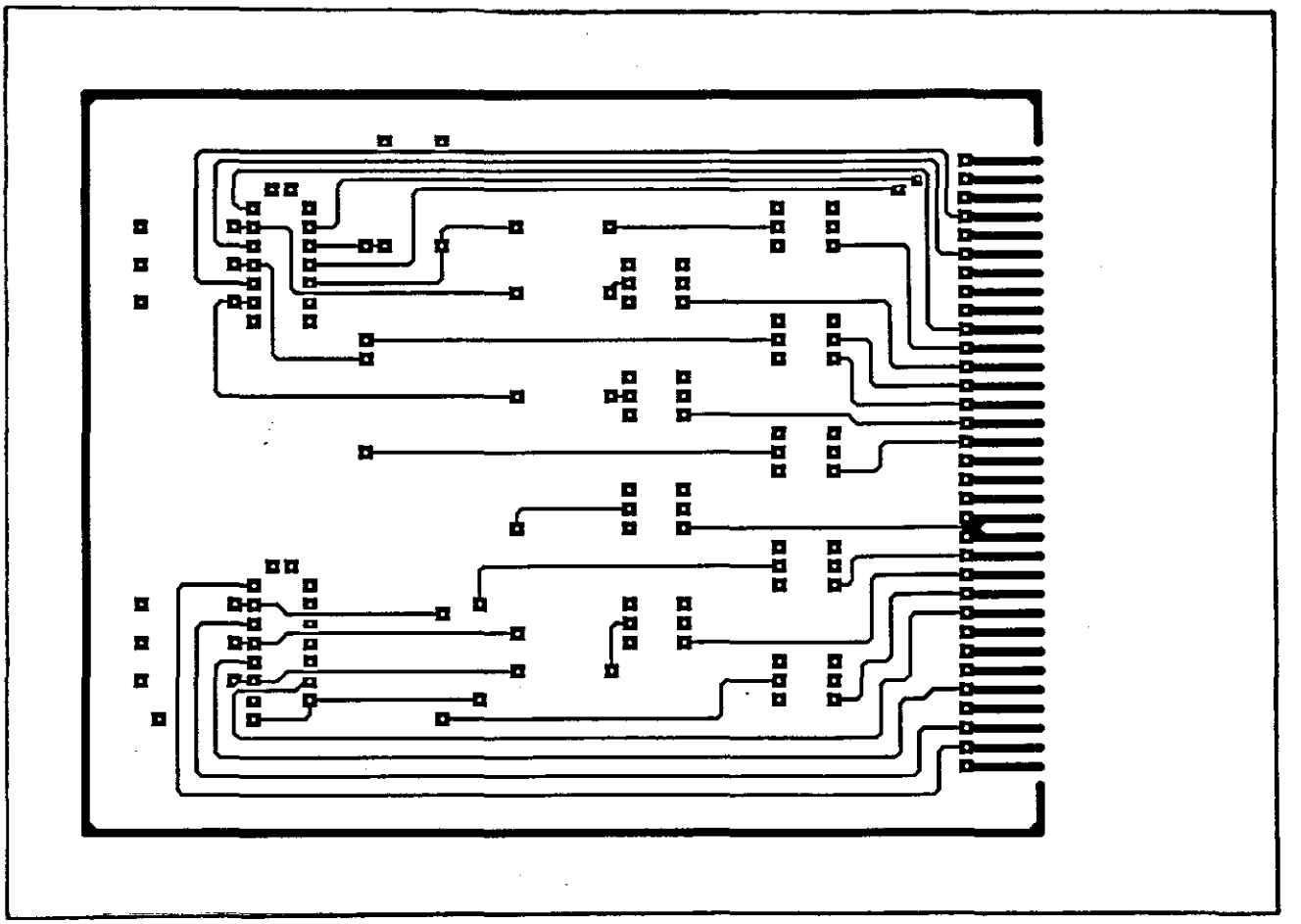


Fig 2.4.5.3 PC board layout (solder side) of Driver Interface module.

2.5 DISPLAY INTERFACE MODULE:

2.5.1 CIRCUIT DESCRIPTION:

The basic functions of this module (fig 2.5.2) are;

(a) It's an interface between the test card and the Display unit.

(b) It stores the fast pulses received from the test card and stretches it so that the pulses is visible on the Display unit.

Resistors (R1 to R10) are used to limit the current to the led's on the Display module.

The basic working of this module is as follow; The complete module can be divided into smaller sections which consists of a couple of diodes, resistors etc. on the input. A D-Type Flip/Flop and a driver output stage (IC5 and IC7). If a short pulse of ± 6 μS is received it will be stored in the D-Type F/F. The output of the F/F will then go high until the RAZ pulse of 64 μS is received at the CLR pin to reset it. The circuitry will automatically be reset every second. The input circuitry of the smaller sections will be different, but this is mainly due to the different output circuitries of the test card.

The purpose of the Diodes (D1,D3,D5,D7....1N4004) are mainly to absorb the higher input (more positive than Vcc .. ± 20V) before it reaches the F/F's inputs and destroys it. The coils which are being used at the output stage of the test card are mainly responsible for the higher input spikes.

Six outputs are tapped from this module to be compared by the Comparator module. The other outputs are send to the Display unit to be displayed.

2.5.2 CIRCUIT DIAGRAM:

See figure 2.5.2 for the circuit diagram of the Display Interface module.

2.5.3 COMPONENT LIST:

RESISTORS:

R1	2K2	1 W
R2	2K2	1 W
R3	1 KΩ	1 W
R4	2K2	1 W
R5	2K2	1 W
R6	2K2	1 W
R7	2K2	1 W
R8	2K7	1 W
R9	2K2	1 W
R10	2K7	1 W
R11	220 Ω	¼ W
R12	220 Ω	¼ W
R13	220 Ω	¼ W
R14	220 Ω	¼ W
R15	220 Ω	¼ W
R16	220 Ω	¼ W
R17	220 Ω	¼ W
R18	220 Ω	¼ W
R19	220 Ω	¼ W
R20	2K2	¼ W
R21	2K2	¼ W
R22	2K2	¼ W
R23	2K2	¼ W
R24	2K2	¼ W
R25	2K2	¼ W
R26	2K2	¼ W
R27	2K2	¼ W
R28	2K2	¼ W
R29	1 KΩ	½ W
R30	470 Ω	¼ W
R31	470 Ω	¼ W
R32	470 Ω	¼ W
R33	470 Ω	¼ W
R34	360 Ω	¼ W
R35	4K7	¼ W
R36	470 Ω	¼ W
R37	470 Ω	¼ W
R38	470 Ω	¼ W
R39	470 Ω	¼ W
R40	1 KΩ	¼ W
R41	1 KΩ	¼ W
R42	1 KΩ	¼ W
R43	1 KΩ	¼ W
R44	1 KΩ	¼ W

DIODES:

D1	1N4007	
D2	1N4148	
D3	1N4007	
D4	1N4148	
D5	1N4007	
D6	1N4148	
D7	1N4007	
D8	1N4148	
D9	1N4148	
D10	4V7	¼ W
D11	1N4007	
D12	1N4007	
D13	1N4007	
D14	1N4007	
D15	1N4148	
D16	1N4148	
D17	1N4148	
D18	1N4148	

CAPACITORS:

C1	33 uF	16 V TAN.
C2	1 uF	16 V TAN.

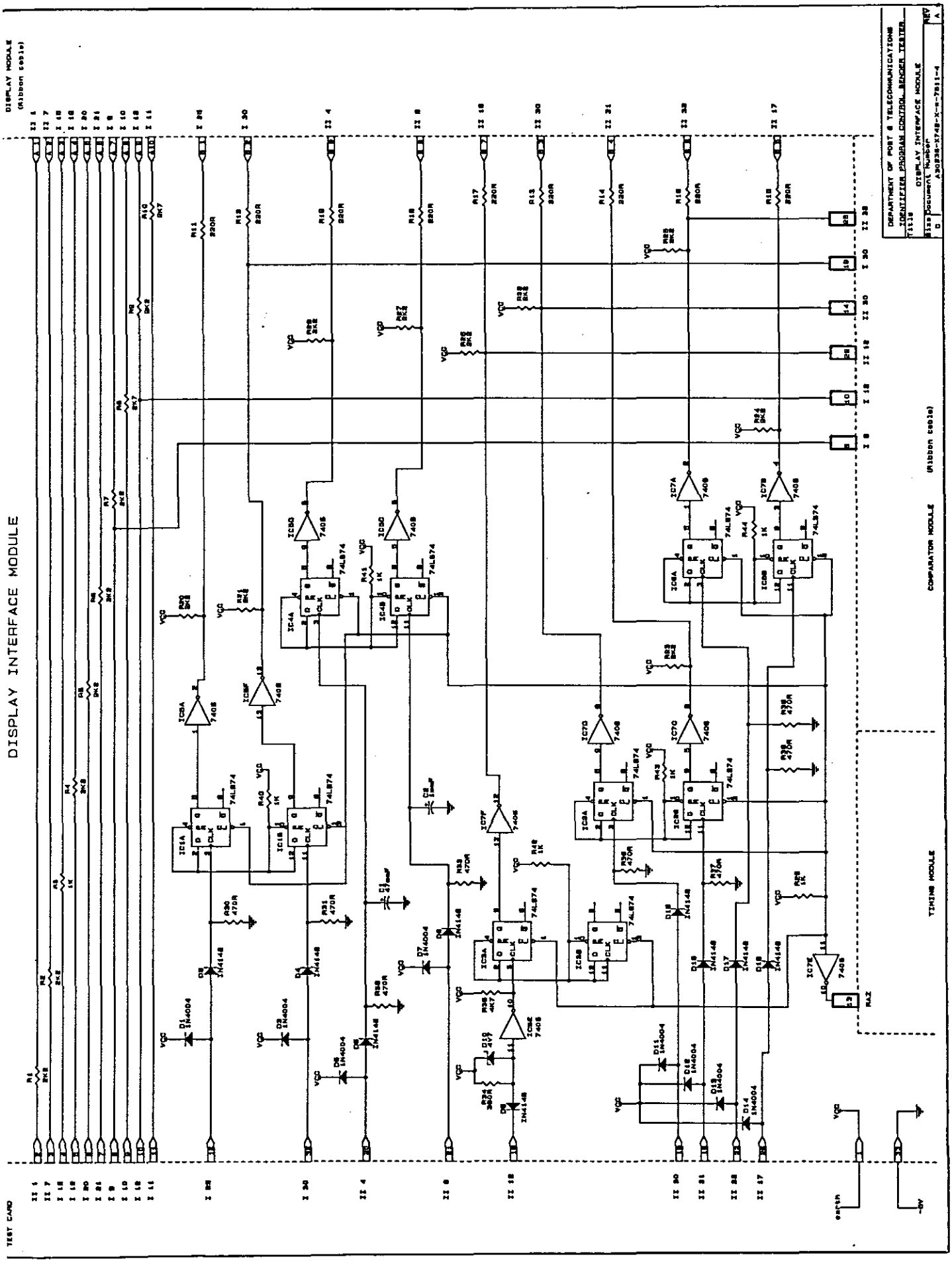
IC's:

IC1	74LS74
IC2	74LS74
IC3	74LS74
IC4	74LS74
IC5	7406
IC6	74LS74
IC7	7406

2.5.4 PRINTED CIRCUIT BOARD LAYOUT:

See figure 2.5.4.1 for the silk screen layout, figure 2.5.4.2 for the component side layout and figure 2.5.4.3 for the solder side layout of the Display Interface module.

Fig 2.5.2 Circuit diagram of Display Interface module.



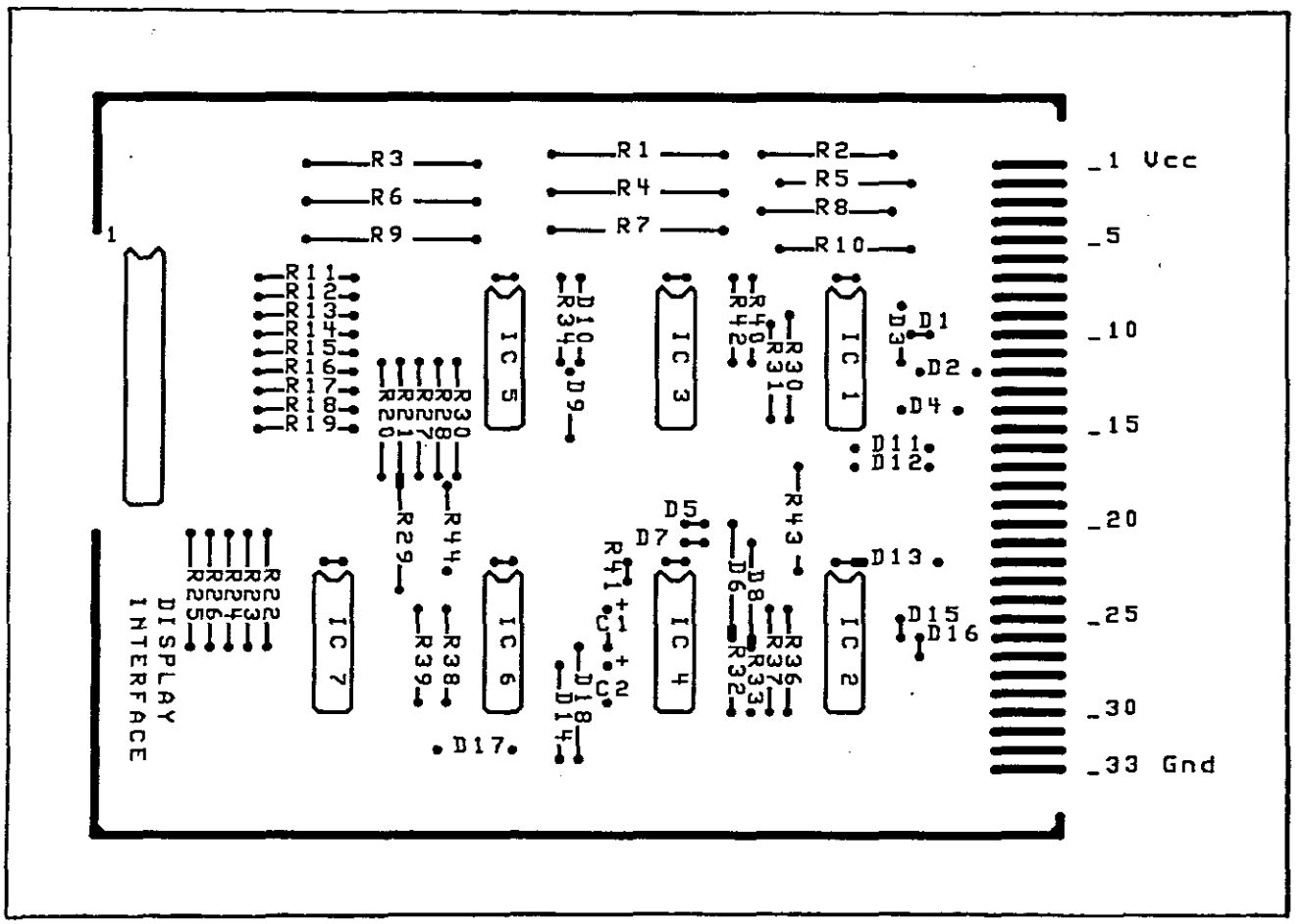


Fig 2.5.4.1 PC board layout (silk screen) of Display Interface module.

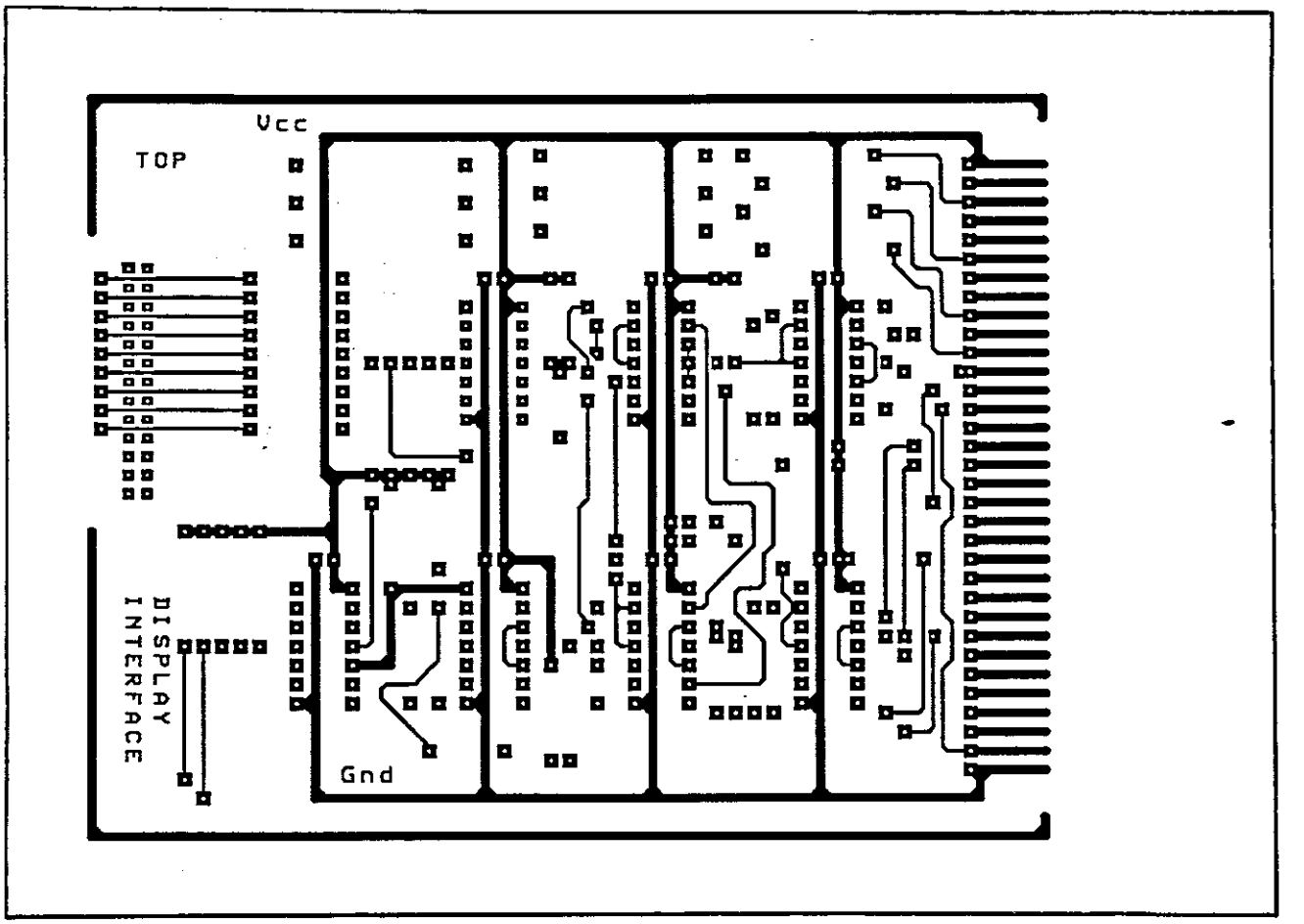


Fig 2.5.4.2 PC board layout (component side) of Display Interface module.

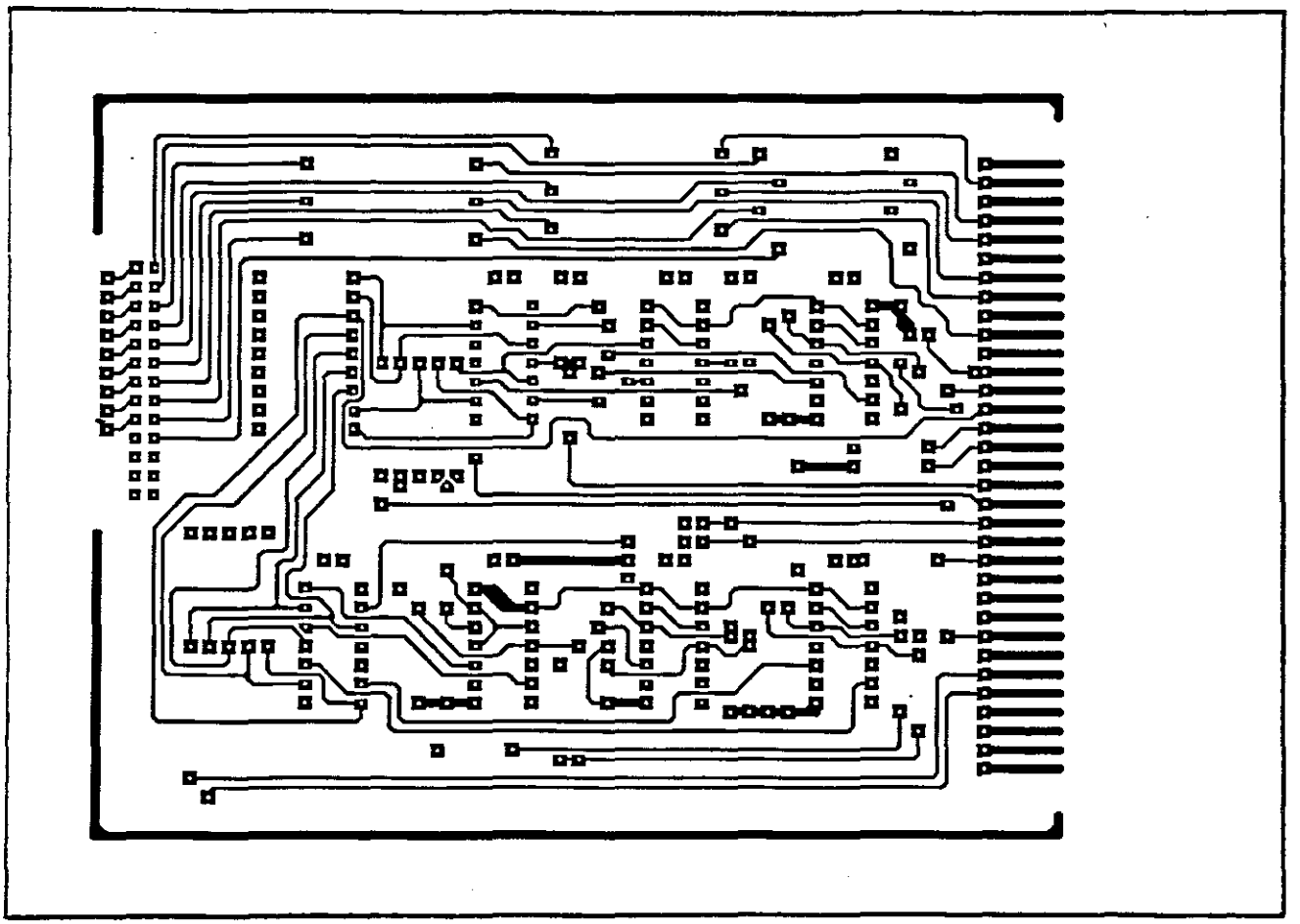


Fig 2.5.4.3 PC board layout (solder side) of Display Interface module.

2.6 DISPLAY UNIT:

2.6.1 CIRCUIT DESCRIPTION:

The only components being used on this unit (fig 2.6.2) are 38 normal red led's and 6 bi-polar led's. Nineteen (D1 to D19) of the red led's are used to display the Reference cards (ID card) outputs, where the other nineteen (D20 to D38) red led's display the Unit Under Test (U.U.T), or Faulty cards outputs.

The Bi-polar led's are mainly used to indicate the different conditions between the two outputs (the Reference card compared to the Unit Under Test). Six outputs of both cards are compared at the same time and displayed on led's D39 to D44. If the outputs compared ok, the led will show "green", where if their did not compared ok, the led will show "red".

On the "Program Control and Impulse Sender" card are eight potentiometers which the technician can adjust to set-up certain timing outputs. This six bi-polar led's will indicate to the repair technician if the timing of the two cards are the same. If the timing are not similar to each other the output sequence of the two cards will be totally different and it will indicate as a fault.

This comparator method should not being used as a final adjustment because its not accurate enough for exchange conditions. The sequence of adjusting the potentiometers on the ID card is as follows;

first Set rotary switch to position 4 and adjust R9 until output I9 only, glows green.
second Set rotary switch to position 3 and adjust R62 until output of I30 only, glows green.
third Set rotary switch to position 4 and adjust R31 until output I12 only, glows green.

This "green/red" indication is then mainly used as a repair aid and not for adjusting.

2.6.2 CIRCUIT DIAGRAM:

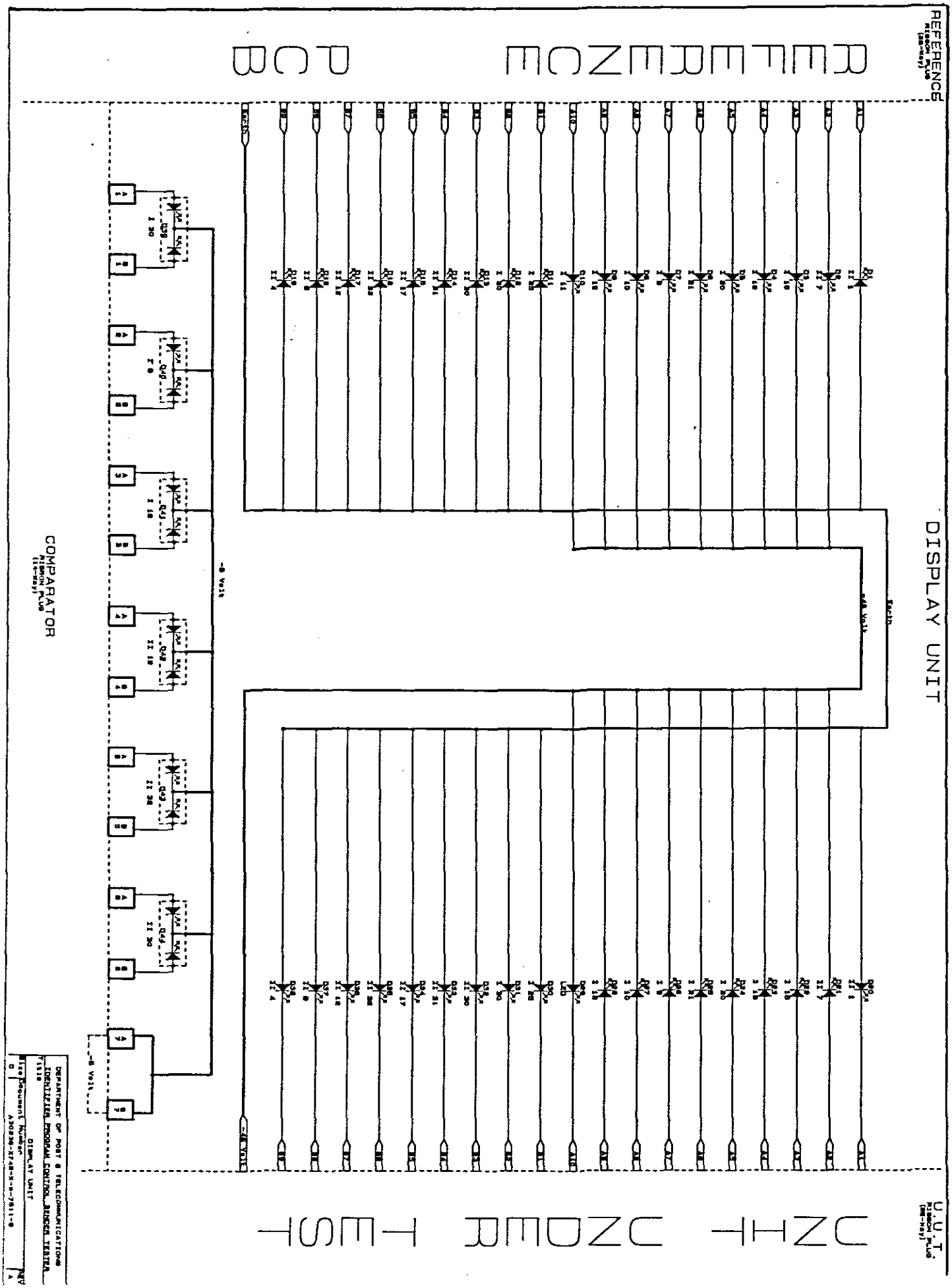
See figure 2.6.2 for the circuit diagram of the Display unit.

2.6.3 COMPONENT LIST:

LED DIODES:

D1 to D38	Red led.
D39 to D44	Bi-colour (com. cathode).

Fig 2.6.2 Circuit diagram of Display unit.



2.7 COMPARATOR MODULE:

2.7.1 CIRCUIT DESCRIPTION:

This module (fig 2.7.2) can be divided into six smaller sections. One output of each card (Ref. Card and U.U.T) is connected to the inputs of a exclusive-or gate (IC1 & IC2). If the two inputs on the exclusive-or are equal the output will be a "low" (green led glows), but if the inputs are different the output will be "high" (red led glows). The output of this gate goes to a inverter and to a bilateral switch (4066). The input of this bilateral switch is connected to "Vcc", making sure that when a "high" appears on it's control line it will switch a "high" through. The inverter stops the two switches from having the same potential on it's control lines, and therefore only one of the outputs will be a "high" potential. The output of this bilateral switch is then connected via. 47 Ω resistors to the bi-polar led on the Display unit.

2.7.2 CIRCUIT DIAGRAM:

See figure 2.7.2 for the circuit diagram of the Comparator module.

2.7.3 COMPONENT LIST:

RESISTORS:

R1	47 Ω	¼ W
R2	47 Ω	¼ W
R3	47 Ω	¼ W
R4	47 Ω	¼ W
R5	47 Ω	¼ W
R6	47 Ω	¼ W
R7	47 Ω	¼ W
R8	47 Ω	¼ W
R9	47 Ω	¼ W
R10	47 Ω	¼ W
R11	47 Ω	¼ W
R12	47 Ω	¼ W
R13	1 KΩ	¼ W
R14	1 KΩ	¼ W
R15	1 KΩ	¼ W
R16	1 KΩ	¼ W

IC's:

IC 1	74LS86
IC 2	74LS86
IC 3	74LS04
IC 4	4066
IC 5	4066
IC 6	4066

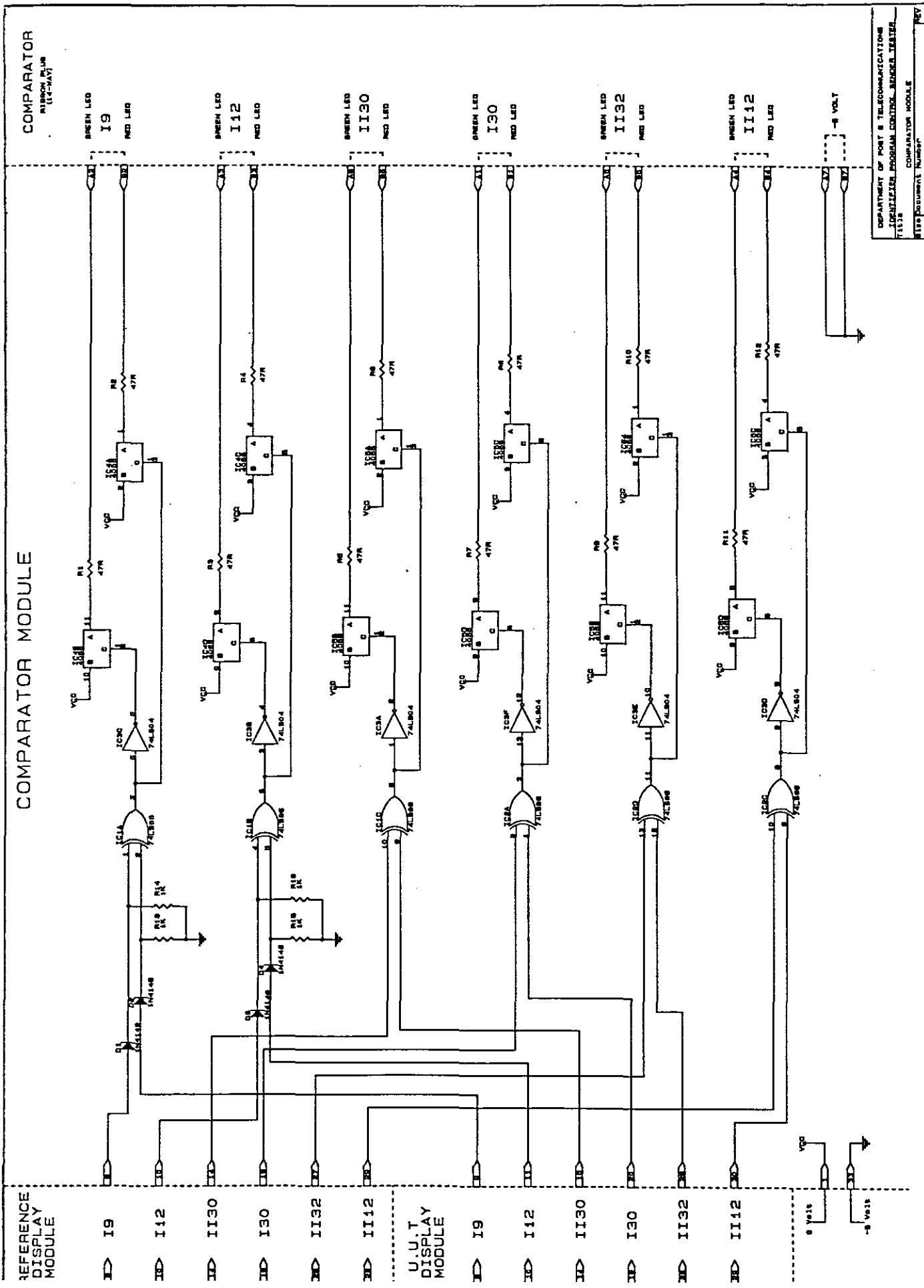
DIODES:

D1	1N4148
D2	1N4148
D3	1N4148
D4	1N4148

2.7.4 PRINTED CIRCUIT BOARD LAYOUT:

See figure 2.7.4.1 for the silk screen layout, figure 2.7.4.2 for the component side layout and figure 2.7.4.3 for the solder side layout of the Comparator module.

Fig 2.7.2 Circuit diagram of Comparator module.



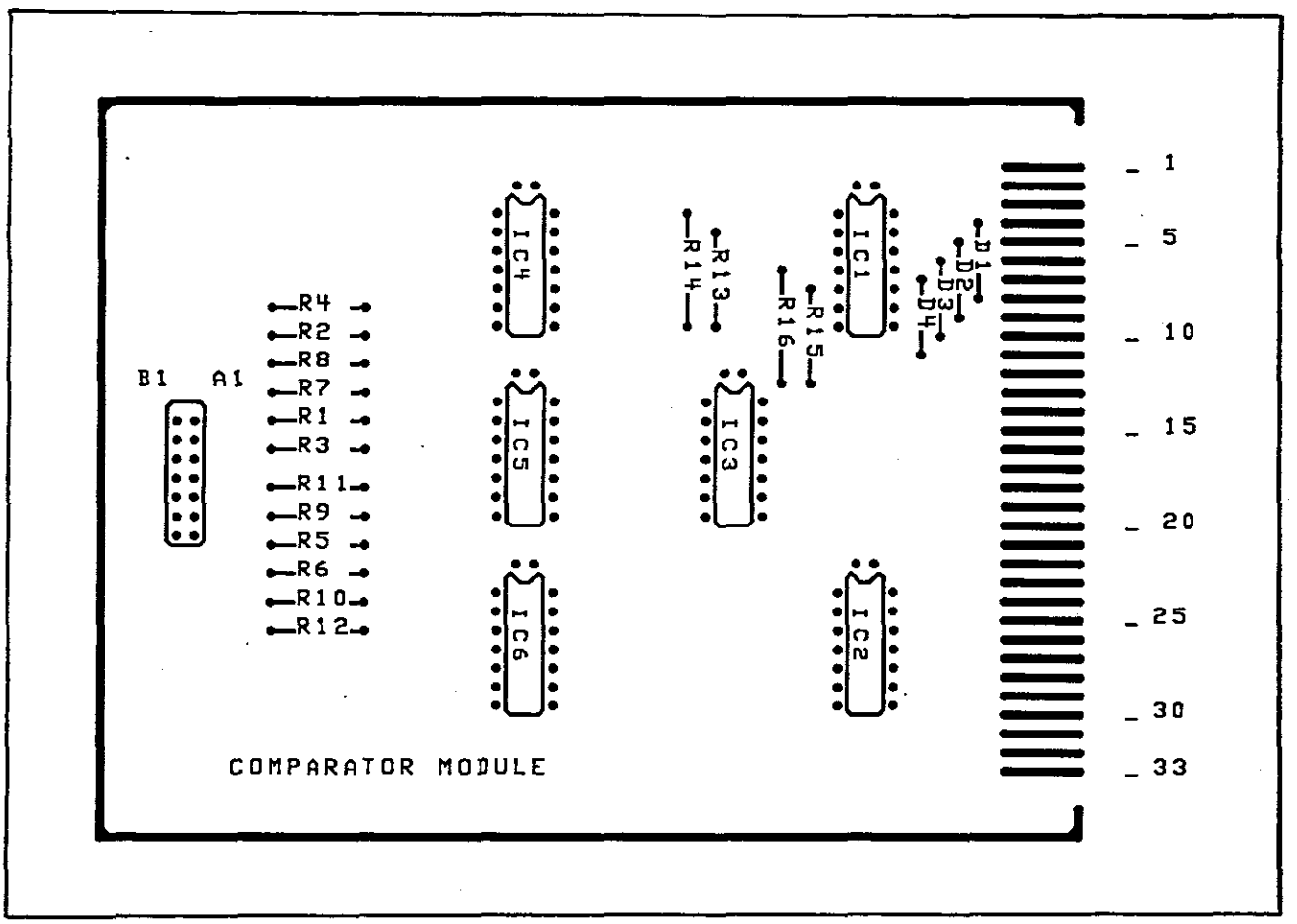


Fig 2.7.4.1 PC board layout (silk screen) of Comparator module.

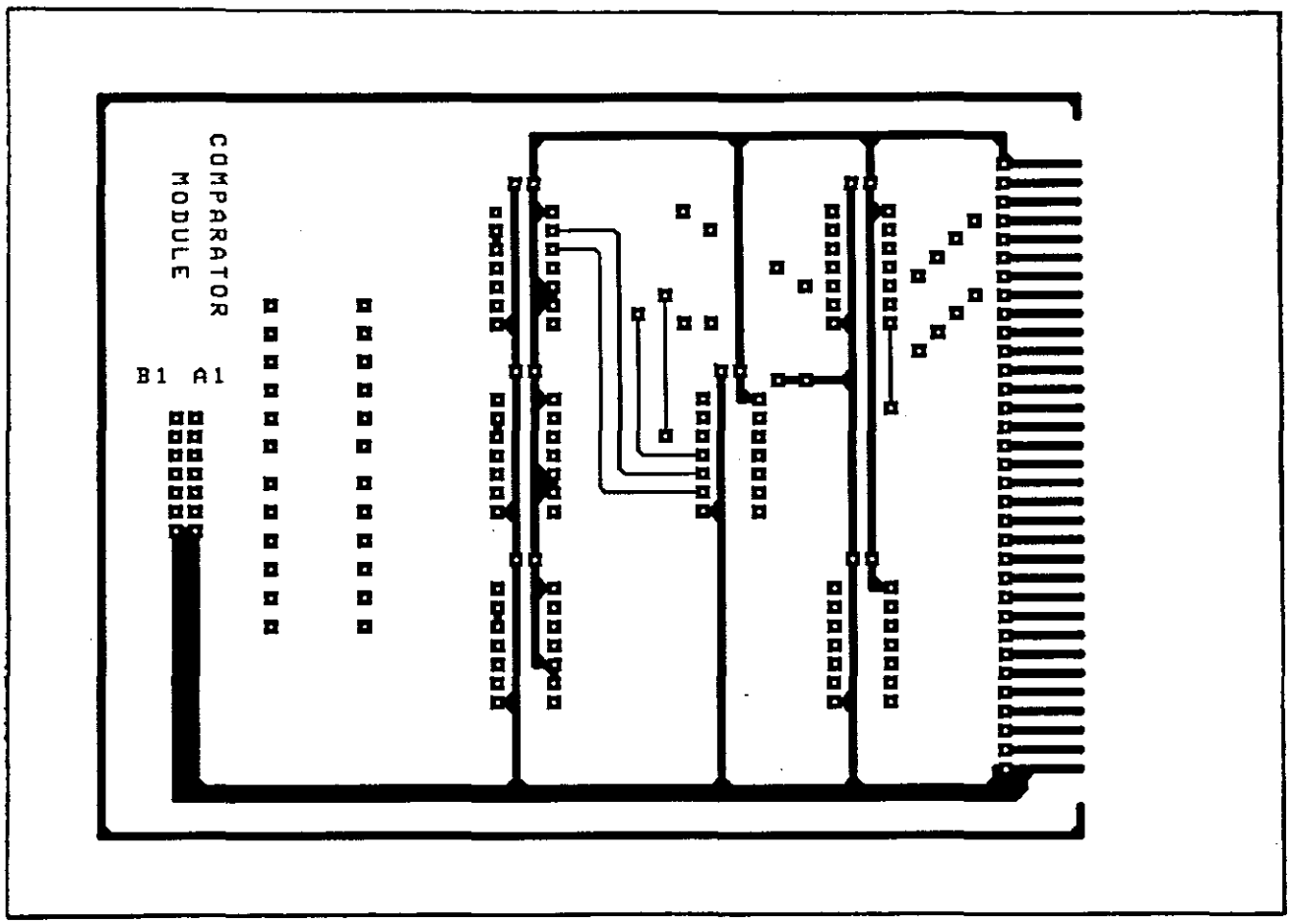


Fig 2.7.4.2 PC board layout (component side) of Comparator module.

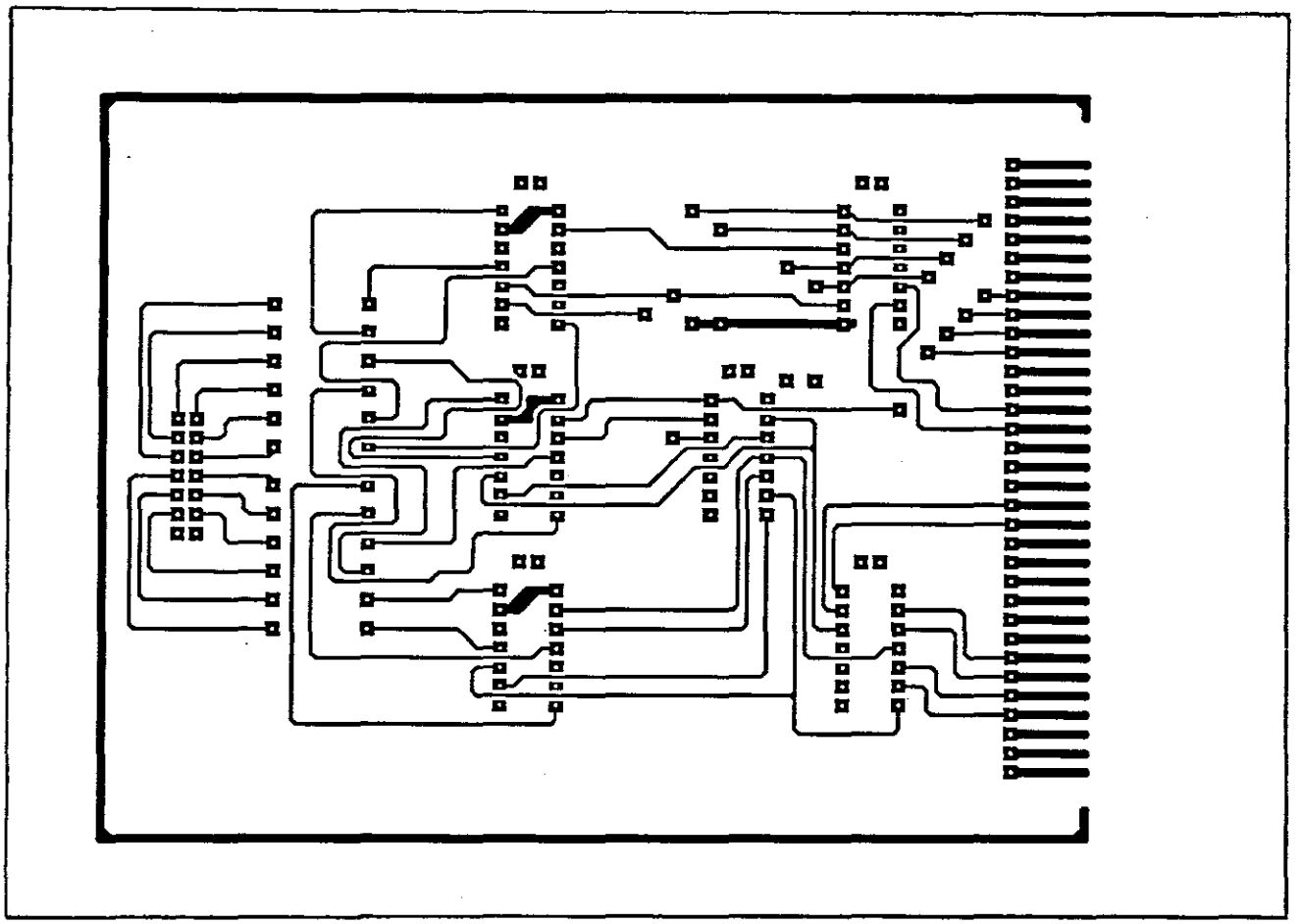


Fig 2.7.4.3 PC board layout (solder side) of Comparator module.

2.8 POWER MODULE:

2.8.1 CIRCUIT DESCRIPTION:

The Power module (fig 2.8.2) supplies -5 Volt/3 Amp and -48 Volt/1 Amp. The -5 Volt supply is used to feed the ID tester and the bi-polar leds on the Display unit. The -48 Volt supply is used to feed the reference card, the faulty card and some of the leds on the Display module.

The "0 Volt" output will be the positive (Vcc) supply, and the "-5 Volt" will be the "ground" supply for the modules in the tester. The " Program Control and Impulse Sender " card functions in the exchange on the basic -48 Volt supply, and therefore this supply was chosen for this Tester.

The Transformer is a 80 VA transformer with two secondary windings.

Winding 1 : 10 Volt/3 Amp rms.
Winding 2 : 50 Volt/1 Amp rms.

Diodes(D1-D4) rectify the 10 V/3 A to a DC potential which is then connected to the 5 V/3 A regulator (IC 1). Diodes (D5-D8) rectify the 50 V/1 A to a DC potential which is then connected to regulator IC2 (connected here as a current limiter). The s.o.t resistor will be selected when the tester is completely built and both cards (Ref. plus UUT) are connected to this supply. The first value was 1,2Ω, which limits the current to a 1 Amp output. Later on this resistance is decreased to allow the cards to draw more current, especially for very short time intervals, when all the led's are light. This current regulated output is then fed to the second regulator (IC 3). IC3's output can be set by adjusting R3 to the specific output voltage required. This combination of R2, R3 and R4 will allow for a swing between 35 Volt and 56 Volt.

The three regulators are mounted on a heat sink which has a thermal resistance of 2,5 deg. Celsius/W.

Calculations: IC 1 input .... ± 14 Volt (11,5 Volt)
IC 1 output ... 5 Volt
At 3 Amp a heat dissipation of 27 Watts maximum. (19,5 W)

IC 3 input.... ± 70 Volt (59 Volt)
IC 3 output... 48 Volt
At 1 Amp, 22 Watts (maximum) must be dissipated. (11 W)

Total of 49 Watt to be dissipated at maximum current. (30 W)

If room temperature is 22 deg. Celsius then the maximum temperature of the heat sink will be ± 145 deg. Celsius.

Please Note: Quantities in brackets are measured quantities on the tester and not theory.

Temperature tests performed on this heat sink under maximum load after one hour prove that with a room temperature of 20 deg. Celsius the heat sink's temperature was 48 deg. Celsius.

2.8.2 CIRCUIT DIAGRAM:

See figure 2.8.2 for the circuit diagram of the Power Supply module.

2.8.3 COMPONENT LIST:

RESISTORS:

R1	s.o.t.	± 0.8 Ω ... 5 W
R2	3K3	½ W
R3	1 KΩ	Lin.pot. (10-turn)
R4	100 Ω	½ W

CAPACITORS:

C1	100 nF	
C2	10000 uF	25 V -- Electrolitic
C3	100 nF	
C4	100 nF	
C5	4700 uF	100 V -- Electrolitic
C6	100 nF	

DIODES:

D1	1N5404	3 Amp
D2	1N5404	3 Amp
D3	1N5404	3 Amp
D4	1N5404	3 Amp
D5	1N5404	3 Amp
D6	1N5404	3 Amp
D7	1N5404	3 Amp
D8	1N5404	3 Amp

IC's:

IC 1	LM323K 5V/3A	
IC 2	LM317T Adj. Regulator/1A	
IC 3	LM317T Adj. Regulator/1A	

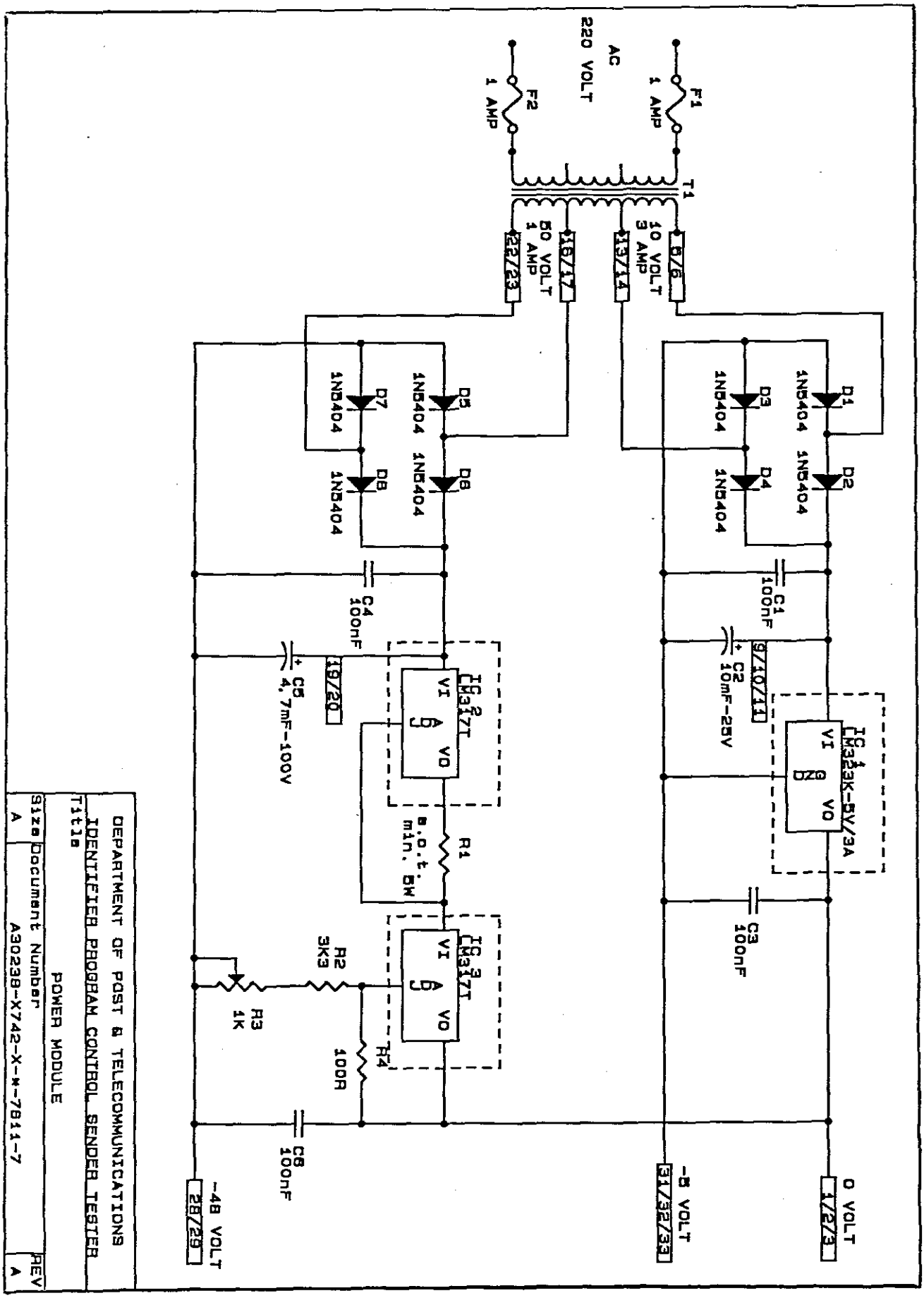
MISCELLANEOUS:

T 1	Transformer 80VA	(first tapping .. 10V/3A) (second tapping .. 50V/1A)
F 1	Fuse	250V/1A
F 2	Fuse	250V/1A

2.8.4 PRINTED CIRCUIT BOARD LAYOUT:

See figure 2.8.4.1 for the silk screen side layout, figure 2.8.4.2 for the component side layout and figure 2.8.4.3 for the solder side layout of the Power Supply module.

Fig 2.8.2 Circuit diagram of Power module.



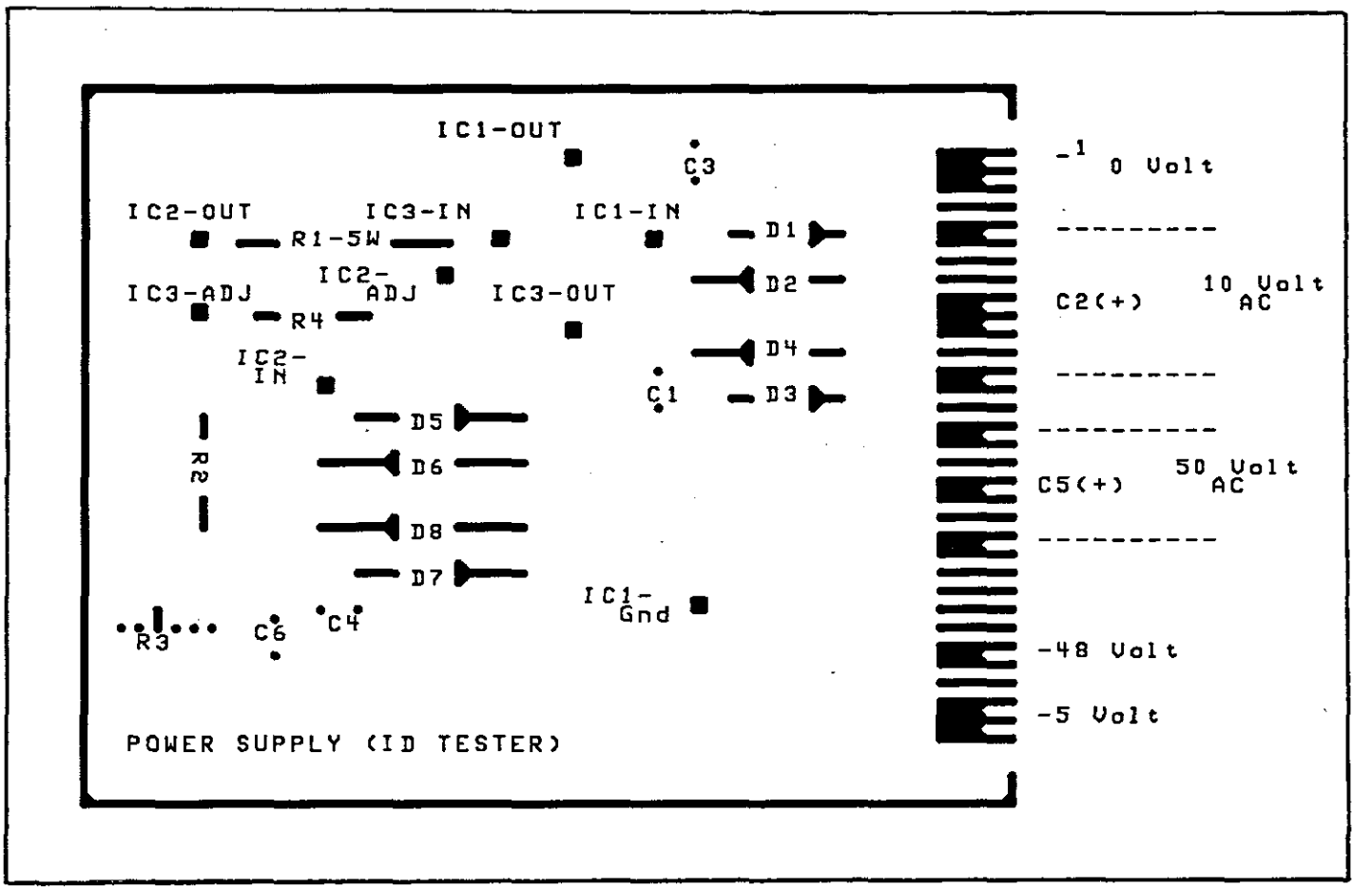


Fig 2.8.4.1 PC board layout (silk screen) of Power module.

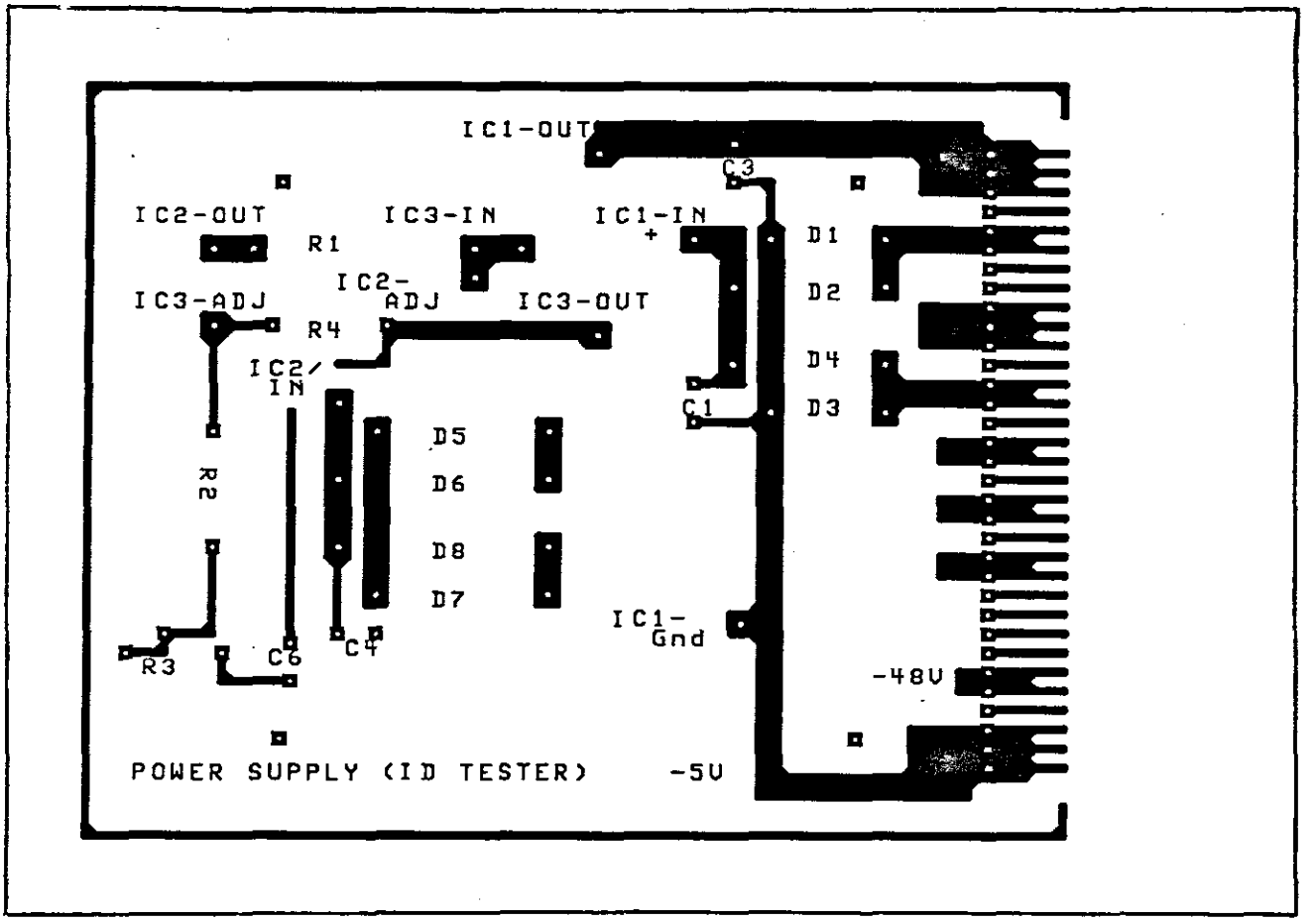


Fig 2.8.4.2 PC board layout (component side) of Power module.

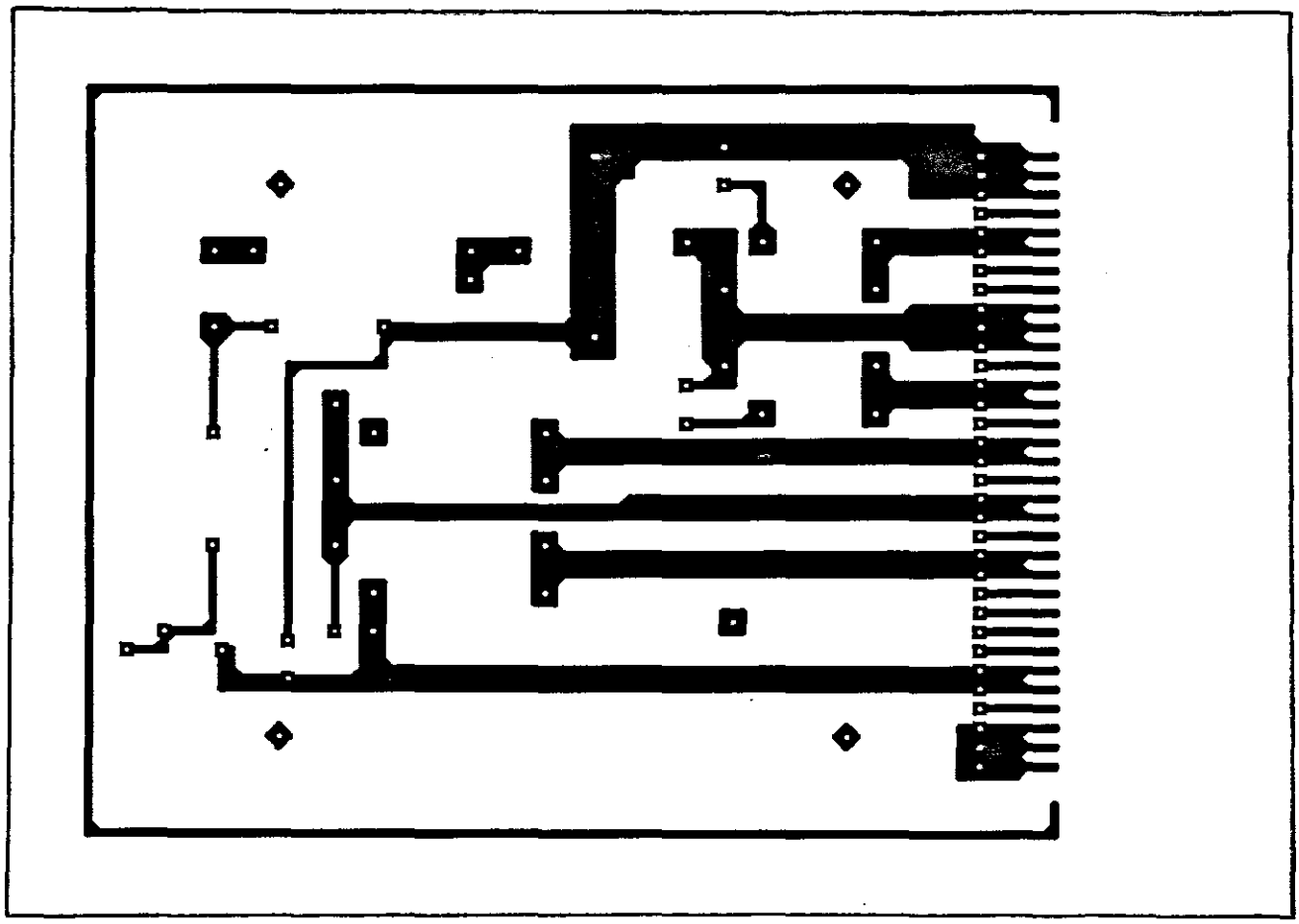


Fig 2.8.4.3 PC board layout (solder side) of Power module.

3.0 TESTING:

3.1 MODIFICATIONS:

The following modifications have taken place during the development period of the ID tester.

* A 8 MHz crystal/resonator is being used in the Timing module presently to generate the master clock. The previous clock used the propagation delay of the 7414 to generate the master clock of ±8 MHz. This wasn't very effective because as soon as the 7414 is replaced with a new one the clock frequency changed.

* Presently a rotary switch is used to split the test procedure into smaller test groups. Previously the test procedure caused a lot of interference due to the timing of the input signals.

* Open-collector drivers are also inserted on the Pulse Sender module to improve the drive ("fanout") capabilities of the varies signals.

* Diodes (D1, D3, D5, D7, etc.) were added on the Display Interface module to protect the input circuitry from the over-shoot input potentials. (± 20 Volt more positive than Vcc). Previously the input circuitry failed after a few minutes in operation.

3.2 COMMISSIONING:

The ID tester was partly tested during November 1988 by using it to repair Identifier cards in the National Electronic Repair Centre. At this stage in time the Comparator card wasn't developed yet in the ID tester. Twenty of the faulty cards were being tested and eighteen of them (the ones that failed only) were repaired by the technicians. The other two cards have being tested and repaired in March 1989 when the ID tester was basically completed. At this time another three Identifier cards were also tested and repaired.

The Identifier tester will be in full service from May 1989.

4.0 CONCLUSION:

The technicians claim that it's now must easier to locate faults on the Identifier cards than previously. It's not boring any more and it's much more satisfying and efficient than the previous method.

The ID tester thus has the following advantages:

* Much improved test and repair procedure.

* Saving on labour (repair) time, thus a saving in costs.

* Improved turn-around time of faulty cards and down-time of system.

* More work satisfaction during testing and repairing of cards.

* No special or expensive equipment required for testing.

5.0 **REFERENCE:**

1.0 **Electronic Identifier and Associated Documents**, by SIEMENS AKTIENGESELLSCHAFT (A30078-X5365-X-26-7618), translated by N Fg SD2/PH, Munich, September 29, 1972.

2.0 **CMOS DATABOOK**, National Semiconductor Corporation.

3.0 **TTL DATABOOK**, TEXAS INSTRUMENTS.

4.0 **LINEAR DATABOOK**, National Semiconductor Corporation.

5.0 **IC MASTER**, by Hearst Business Communications.

6.0 **Designing with TTL Integrated Circuits**, by McGraw-Hill's TEXAS INSTRUMENTS ELECTRONICS SERIES,